Integrated RF Power Amplifier Design in Silicon-Based Technologies

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Abstract

This thesis presents the design and implementation of the RF power amplifiers in modern silicon based technologies. The main challenge is to include power amplifier on a single chip with output power level in watts, operating at high frequencies where the transit frequency (f_T) is just a few times higher than the operating frequency.

This work describes the design procedure for bipolar and CMOS transformer-based Class-A, Class-AB and Class-B power amplifiers. The design procedure is based on the HICUM for bipolar and BSIM4 for CMOS transistor models and is divided in four parts:

- Building a one transistor prototype power amplifier which is based on the analytical analysis of the output characteristics and transistor model.
- Load-pull simulation to define the final input and output impedances.
- Derivation of the analytical equations for the transformer-based matching network.
- Design of the final transformer-based push-pull power amplifier.

A good agreement between the proposed analytical analysis and large-signal (harmonic balance) simulation results proofs usefulness of the proposed power amplifier design approach. Additionally, it shows the contribution of the separated devices at the final design that helps to find a technology limits in the current circuit design.

The main achievements include:

- A 2.4 GHz power amplifier in 0.13 μm CMOS technology. An output power of 28 dBm is achieved with a power added efficiency of 48 % at a supply voltage of 1.2 V [Vasylyev 04].
- Two 17 GHz power amplifiers in 0.13 μm CMOS technology (one fully integrated while the other with external matching network) with output power exceeding 50 mW. The former exhibits a power added efficiency of 9.3 % while the latter a 15.6 % power added efficiency [Vasylyev 06].
- A fully integrated K and Ka bands power amplifier in 0.13 μm CMOS technology. A 13 dBm output power along with power added efficiency

of 13 % is achieved at an operating frequency of 25.7 GHz with 1.2 V supply [Vasylyev 05,a].

- A fully integrated power amplifier based on a novel power combining transformer structure in 28 GHz-f_T SiGe-bipolar technology. A 32 dBm output power along with power added efficiency of 30 % is achieved at an operating frequency of 2.12 GHz with 3.5 V supply [Vasylyev 05,b].

Zusammenfassung

Diese Doktorarbeit beschäftigt sich mit dem Entwurf und der Ausführung von Hochfrequenz-Leistungsverstärkern in modernen Silizium Technologien. Die Herausforderung ist, HF-Leistungsverstärker mit mehreren Watt Ausgangsleistung vollständig monolithisch zu integrieren; wobei die Betriebsfrequenz bereits 25 % der Transitfrequenz (f_T) beträgt.

Diese Arbeit beschreibt das Entwurfverfahren für bipolar und CMOS Leistungsverstärker der Klasse-A, Klasse-AB und Klasse-B mit monolithisch integrierten Transformatoren. Das Entwurfverfahren verwendet für bipolar das HICUM Transistor-Modell und für CMOS das BSIM4 Transistor-Modell und lässt sich in vier Teile gliedern:

- Analyse eines Ein-Transistor-Verstärkers, basierend auf der analytischen Analyse der Ausgangcharakteristiken und der Transistor-Modelle.
- Simulation mit Lastvariation, zur Ermittlung der optimalen Ein-und Ausgangsimpedanzen.
- Ableitung der analytischen Gleichungen für das Transformator Anpassungsnetz.
- Entwurf vom optimierten Gegentaktleistungsverstärker mit monolithischen Transformatoren.

Eine gute Übereinstimmung zwischen der vorgeschlagenen analytischen Analyse und dem Großsignal-Simulationenergebnis beweist die Nützlichkeit der vorgeschlagenen Verstärker-Entwurfannäherung. Zusätzlich zeigt es den Beitrag der einzelnen Komponenten, was das optimale Ausreizen der Technologie ermöglicht.

Die Hauptergebnisse:

- Ein 2.4 GHz Leistungsverstärker in einer 0.13 μm CMOS Technologie mit einer Ausgangsleistung von 28 dBm und einem Verstärkerwirkungsgrad von 48 % an einer Versorgungsspannung von 1.2 V [Vasylyev 04].
- Zwei 17 GHz Leistungsverstärker in einer 0.13 μm CMOS Technologie (eine Variante enthält ein monolithisch integriertes Anpassungsnetzwerk, die andere Variante enthält ein externes Anpassungsnetzwerk) mit einer Ausgangsleistung über 50 mW. Der Verstärkerwirkungsgrad beträgt 9.3 % für Variante 1 und 15.6 % für Variante 2 [Vasylyev 06].

- Ein völlig integrierter K und Ka Band-Leistungsverstärker in einer 0.13 μm CMOS Technologie. Bei einer Betriebsfrequenz von 25.7 GHz wird eine Ausgangsleistung von 13 dBm und ein Verstärkerwirkungsgrad von 13 % erreicht (1.2 V Versorgungsspannung) [Vasylyev 05,a].

- Ein völlig integrierter Leistungsverstärker basierend auf einer neuartigen Transformator-Struktur in einer 28 GHz-f_T SiGe Bipolar Technologie. Eine Ausgangsleistung von 32 dBm und ein Verstärkerwirkungsgrad von 30 % werden bei einer Betriebsfrequenz von 2.12 GHz und 3.5 V Versorgungsspannung erreicht [Vasylyev 05,b].

Contents

List of Abbreviations

AC	*A*lternating *C*urrent
ACPR	*A*djacent *C*hannel *P*ower *R*atio
BALUN	*BAL*anced to *UN*balanced
BICMOS	*B*ipolar *C*omplementary *M*etal *O*xide *S*emiconductor
BJT	*B*ipolar *J*unction *T*ransistor
BSIM	*B*erkley *S*hort-Channel *I*GFET *M*odel
BPSK	*B*inary *P*hase *S*hift *K*eying
BW	*B*ond *W*ire
CBGA	*C*eramic *B*all *G*rid *A*rray
CCDF	*C*omplementary *C*umulative *D*istribution *F*unction
CDF	*C*umulative *D*istribution *F*unction
CLM	*C*hannel *L*ength *M*odulation
CMOS	*C*omplementary *M*etal *O*xide *S*emiconductor
CPP	*C*omplementary *P*ush-*P*ull
DECT	*D*igital *E*nhanced *C*ordless *T*elecommunications
DFDA	*D*ual-*F*ed *D*istributed *A*mplifier
DHBT	*D*ouble-*H*eterostructure *B*ipolar *T*ransistor
DIBL	*D*rain *I*nduced *B*arrier *L*owering
DITS	*D*rain *I*nduced *T*hreshold *S*hift
DUT	*D*evice *U*nder *T*est
dc	*d*irect *c*urrent
EDGE	*E*nhanced *D*ata rates for *G*lobal *E*volution
E	Drain (Collector) *E*fficiency
EVM	*E*rror *V*ector *M*agnitude
FDMA	*F*requency *D*ivision *M*ultiple *A*ccess
FET	*F*ield *E*ffect *T*ransistor
FI	*F*ully *I*ntegrated
f_{max}	Maximum oscillation frequency in [Hz]
f_T	Transit frequency in [Hz]
GaAs	*Ga*llium *As*enide
GaN	*Ga*llium *N*itride
GMSK	*G*aussian *M*inimum *S*hift *K*eying
GPRS	*G*eneral *P*acket *R*adio *S*ervices
GSM	*G*lobal *S*ystem for *M*obile Communications
HEMT	*H*igh *E*lectron *M*obility *T*ransistor
HBT	*H*eterojunction *B*ipolar *T*ransistor
HICUM	*HI*gh-*CU*rrent *M*odel
HPP	*H*orizontal *P*arallel *P*late
IC	*I*ntegrated *C*ircuit
IGFET	*I*solated-*G*ate *F*ield-*E*ffect *T*ransistor

IMD	*I*nter*M*odulation *D*istance
InP	*In*dium *P*hosphite
IP3	Third order intermodulation point
ISM	*I*ndustrial *S*cientific *M*edical
LDMOS	*L*aterally *D*iffused *M*etal *O*xide *S*emiconductor
LTCC	*L*ow *T*emperature *C*ofired *C*eramics
MEMS	*M*icro-*E*lectro-*M*echanical *S*ystem
MIM	*M*etal-*I*nsulator-*M*etal
MMIC	*M*onolithic *M*illimeter-wave *I*ntegrated *C*ircuit
MN	*M*atching *N*etwork
MSAG	*M*ultifunction *S*elf-*A*ligned *G*ate
MSI	*M*icromachined *S*olenoid *I*nductor
MOS	*M*etal *O*xide *S*emiconductor
OFDM	*O*rthogonal *F*requency *D*ivision *M*ultiplexing
OCM	*O*ff-*C*hip *M*atching
PA	*P*ower *A*mplifier
PAE	*P*ower *A*dded *E*fficiency
PCB	*P*rinted *C*ircuit *B*oard
PSK	*P*hase *S*hift *K*eying
RFC	*R*adio-*F*requency *C*hoke
SCBE	*S*ubstrate *C*urrent *I*nduced *B*ody *E*ffect
SiGe	*Si*licium *Ge*rmanium
SHF	*S*uper *H*igh *F*requency (3 .. 30 GHz)
SPICE	*S*imultion *P*rogram with *I*ntegrated *C*ircuit *E*mphasis
SW	*Sw*itch
TDMA	*T*ime *D*ivision *M*ultiple *A*ccess
TRADICA	*TRA*nsistor *DI*mensioning and *CA*lculation
Tranceiver	*Trans*mitter and re*ceiver*
UHF	*U*ltra *H*igh *F*requency (300 .. 3000 MHz)
VPP	*V*ertical *P*arallel *P*late
VSWR	*V*oltage *S*tanding *W*ave *R*atio
WLAN	*W*ireless *L*ocal *A*rea *N*etwork

Symbol Convention

Throughout the thesis, signals (voltages and currents) are denoted in accordance with:

- Bias and dc quantities: with capital letters and capital indices (e.g. I_C, V_{CE}).
- Total instantaneous voltages and currents: with capital letters and small indices (e.g. I_c).
- Small-signal voltages and currents also elements such as transconductance in small-signal equivalent circuits: with small letters and small indices (e.g. i_c, g_m).

Chapter 1

Introduction

The wireless communication system consists of at least two main blocks such as a transmitter and a receiver. Usually they are combined in one block that is called transceiver (*trans*mitter + re*ceiver*) (see Fig. 1.1).

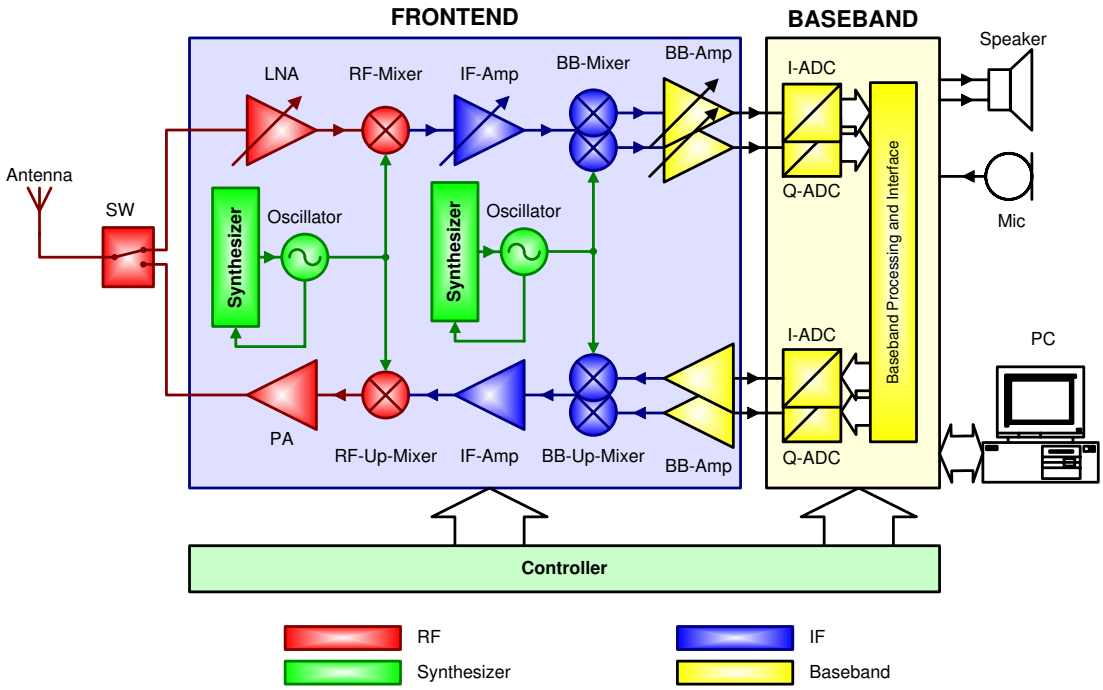


Figure 1.1: Block diagram of a typical wireless digital communications transceiver.

The radio frequency power amplifier is an electrical device which amplifies the input signal by transforming the dc energy of power supply into the output signal. The name "Radio Frequency" indicates that the amplifier operates with radio frequency signals meant for sending through the propagation medium (air, water etc.) by electromagnetic waves and works at frequency range from 3 Hz (submarine's communication) to 300 GHz (radio astronomy). This work is focused at

Ultra High Frequency (UHF) and Super High Frequency (SHF) bands where currently are around one milliard of mobile devices in use. The word "power" means that the amplifier operates with signal levels from a condition when signal levels are less than 1 % of the bias currents and voltages up to a condition when the bias currents or voltages are absent. It is the "last" active device in the transmitter chain and has the highest output power as well as power consumption which vary from a few hundred milliwatts for a cellular phone up to hundreds watts for a base station.

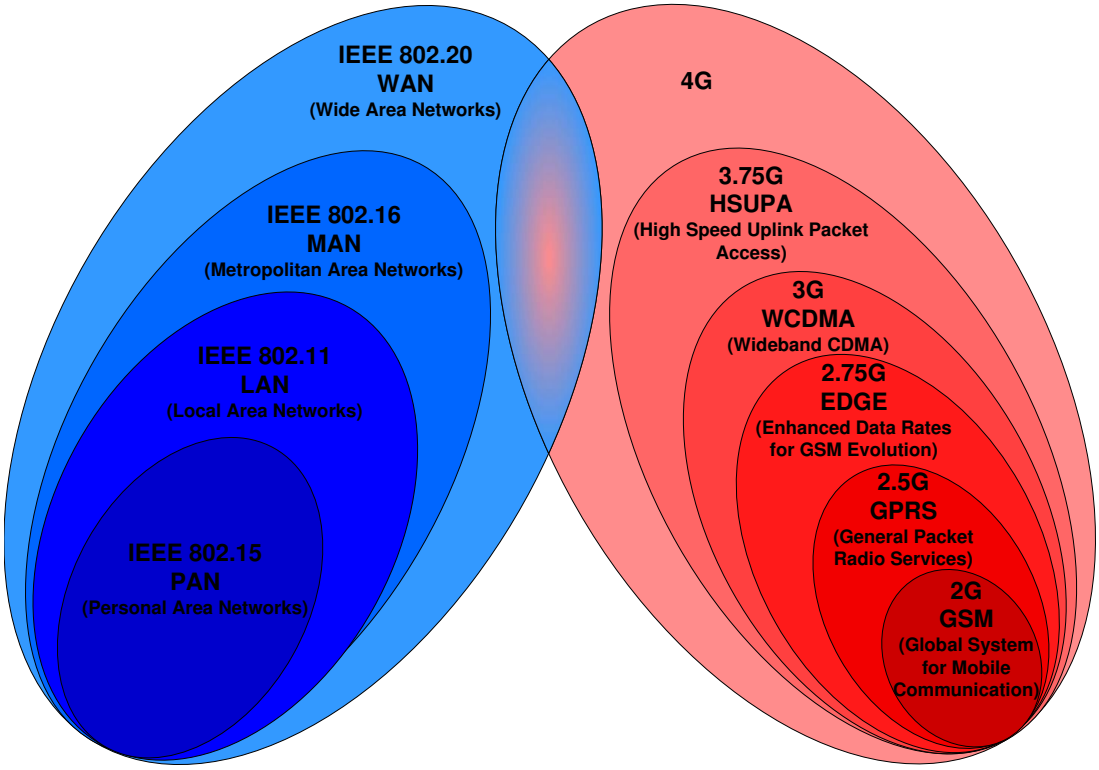


Figure 1.2: Wireless communication standards evolution.

Fig. 1.2 gives an overview of the wireless world evolution, particularly of the wireless local area networks (WLAN) and cellular networks. The key features of standards with typical electrical characteristics of the correspondent power amplifier available on the market are listed in Tables 1.1 and 1.2 for mobile and WLAN technologies. Among them, the operating frequency, output power and modulation define the choice of the power amplifier class, fabrication technology(ies) and level of the integration.

Table 1.1: Mobile technologies.

Standard	**GSM**	**GPRS**	**EDGE**	**WCDMA**	**HSUPA**
Year introduced	1990	2000-2001	2003	2001	2006+
Uplink frequency band (MHz)	Europe890-915	Europe890-915	Europe1920-1980	1920-1980	1920-1980
Carrier spacing (kHz)	200 kHz	200 kHz	200 kHz	5 MHz	5 MHz
Multiple access	TDMA/FDMA	TDMA/FDMA	TDMA/FDMA	CDMA	CDMA
Modulation	GMSK	GMSK	8-PSK	HPSK	HPSK(16QAM?)
Duplex mode	FDD	FDD	FDD	FDD	FDD
Maximum Data Rate	9.6 kbps	14 kbps	118.4 kbps	384 kbps	5.76 Mbps
Typical PA Output Power (dBm)	35.0	35.0		28.0	
Typical PA supply voltage (V)	3.5	3.5	3.5	3.4	
Typical PA ACPR (dBc)	N/A	N/A		> -40@5MHz	
Typical PA quiescent current (mA)	20	20		65	
Typical Efficiency (%)	> 50	> 50	> 20	> 40	

Table 1.2: Wireless LAN technologies.

Standard	**IEEE 802.15.3a**	**IEEE 802.11b**	**IEEE 802.16a**	**IEEE 802.20**
Year introduced	2004-2005	1999	2005	2001
Uplink frequency band (MHz)	3.1-10.6 GHz	2.4-2.435 GHz	2-11 GHz	<3.5 GHz
Carrier spacing (kHz)	>528 MHz	Europe 30(10) MHz	1.25-20 MHz	
Multiple access	CSMA/CA	CSMA/CA	TDMA	under definition
Modulation	Shaped Pulse or Frequency switched OFDM	BPSK, QPSK, (CCK, PBCC)	OFDM with QPSK 16QAM,64QAM	under definition
Duplex mode	TDD	TDD	TDD/FDD	TDD/FDD
Maximum Data Rate	480 Mbps	11 Mbps	75 Mbps	

The Samsung Z500 GSM/WCDMA mobile phone is a good example of a typical wireless system which contains 2G and 3G technologies (see Fig. 1.3). Its active front end consists of Qualcomm RTR6250 WCDMA Tx, GSM TRx; Qualcomm RFR6200 WCDMA Rx; Agilent WCDMA PA Module and Skyworks GSMA PA Module. The Skyworks GSMA PA Module (6 x 6 mm^2) contains a GaAs HBT PA die and a SiBiCMOS controller die plus 27 passives.

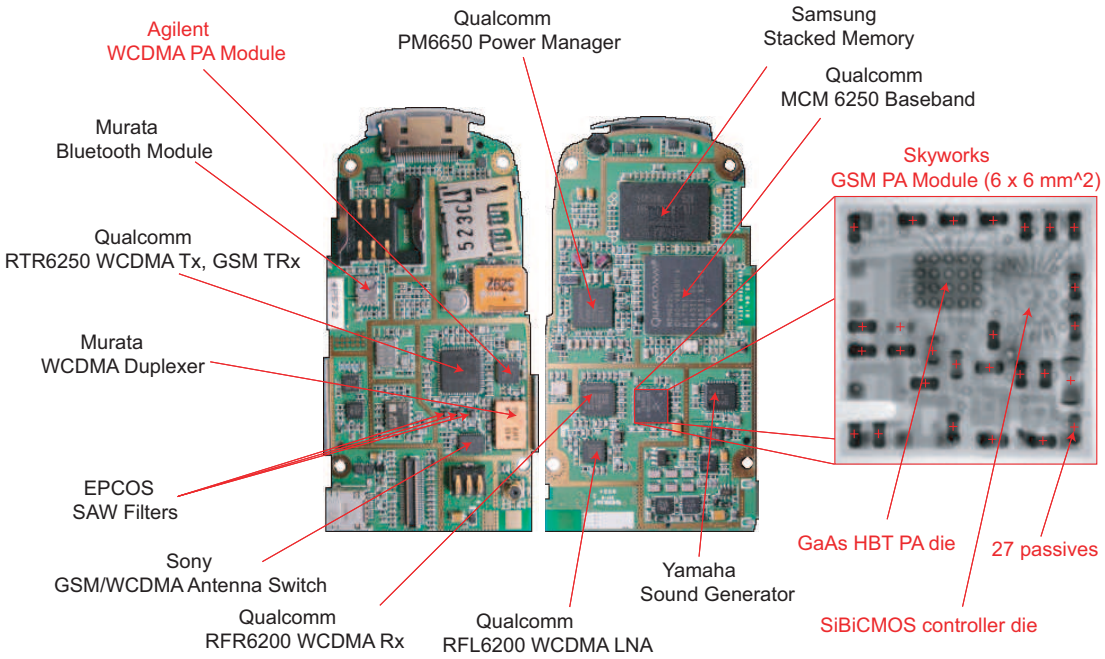


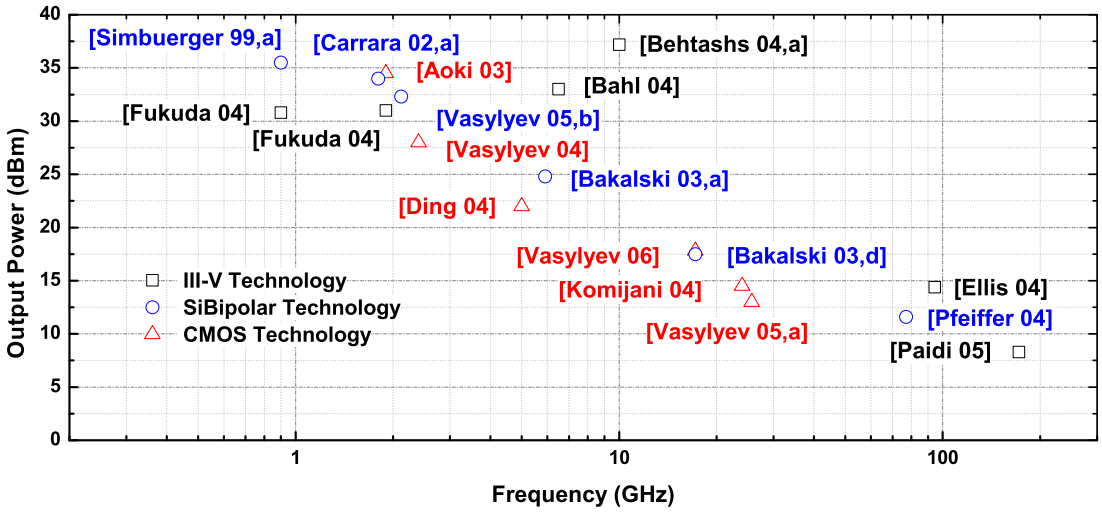
Figure 1.3: Inside Samsung Z500 GSM/WCDMA mobile phone.

Until now, almost all wireless power amplifiers are produced in GaAs technologies and PA modules presented above confirms it. Modern sub-micron Si, SiGe Bipolar and Si CMOS technologies are very attractive from the level of integration point of view. They could integrate all components of a PA module (power amplifier core, control circuits, passives) on one die with further possibility of integration with the RF front-end part as well as with the digital signal processing (DSP) part.

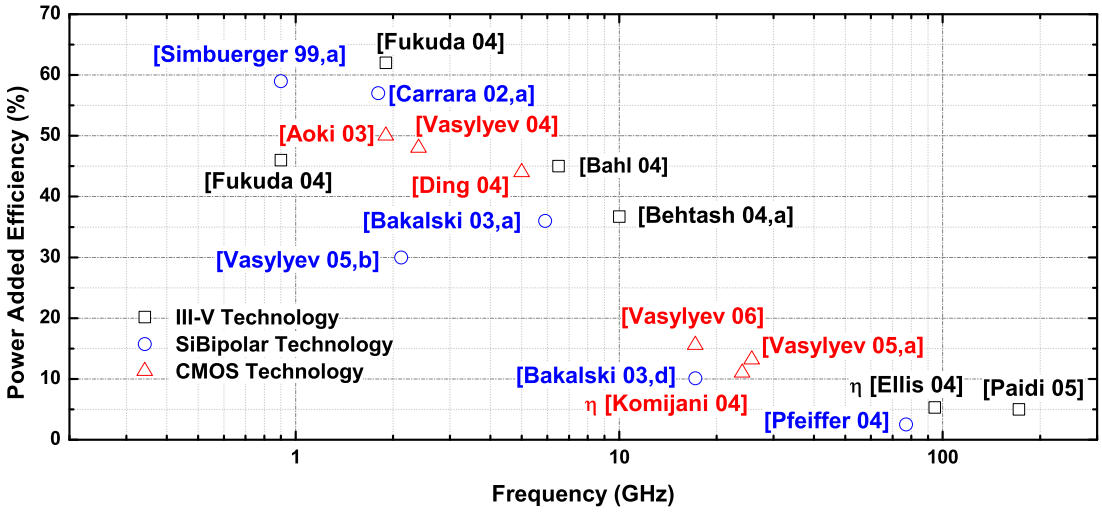
1.1 State of the Art

The interested publications of the last decade are collected and analysed during this work which is sectioned in three parts: the power amplifiers in III - V technologies (see Table A.1), the power amplifier in CMOS technologies (see Table A.2) and the power amplifiers in Si, SiGe - Bipolar technologies (see Table A.3). The most interesting works on the author point of view as well as the own works

are highlighted in Fig. 1.4, showing that the outcome of this work acquires one of the leading position in the existing monolithically integrated power amplifier state of the art.



(a)



(b)

Figure 1.4: Some of recent published works concerning the power amplifier design grouped by: (a) Output power; (b) Power added efficiency.

Chapter 2

Power Amplifier Basics

2.1 Main Characteristics

Consider the generalized single-stage power amplifier circuit diagram in Fig. 2.1 in order to determine the main characteristics of the power amplifier. The circuit diagram consists of a source, an input matching network, an input bias network, an active device, an output bias network, an output matching network and a load. The load can be an antenna, a switch, or a following power amplifier stage in case of a multi-stage power amplifier. The output matching network converts the impedance of the load to impedance that provides proper functionality of the power amplifier. Output and input bias networks provide the operating points for the active devices. An active device can be a single transistor, valve or a composite one. The input matching network converts the input impedance of the active device to impedance that provides proper functionality of the power amplifier. The source can be a signal generator, a previous block of a transmitter or an amplifier stage in case of a multi-stage power amplifier.

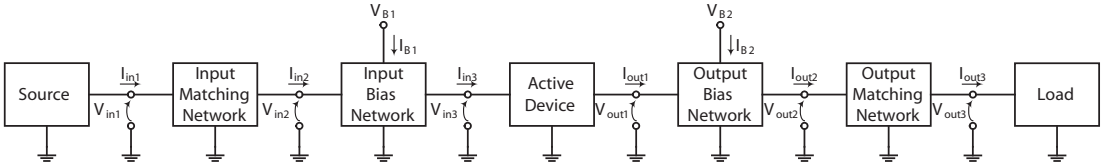


Figure 2.1: Generalized single-stage power amplifier circuit diagram.

2.1.1 Power

Direct Current Power Consumption

The dc power consumption of the power amplifier is defined as:

$$P_{DC} = V_{B1}I_{B1} + V_{B2}I_{B2} \tag{2.1}$$

RF Power

The power delivered to the load is defined as:

$$P_{l,1} = \frac{1}{2}\Re(V_{out3,1}I^*_{out3,1}) \tag{2.2}$$

The power available from the source is given as:

$$P_{avs,1} = \frac{I^2_{s,1}}{8G_{s,1}} \tag{2.3}$$

The input power is expressed as:

$$P_{in,1} = \frac{1}{2}\Re(V_{in1,1}I^*_{in1,1}) \tag{2.4}$$

The power available from the amplifier is:

$$P_{ava,1} = \frac{I^2_{a,1}}{8G_{a,1}} \tag{2.5}$$

2.1.2 Power Gain

The power gain has several definitions: the transducer power gain, the operating power gain, and the available power gain [Gonzalez 97].

The transducer power gain is defined as the ratio of the power delivered to the load to the power available from the source:

$$G_{t,1} = \frac{P_{l,1}}{P_{avs,1}} \tag{2.6}$$

The operating power gain is defined as the ratio of the power delivered to the load to the input power to the amplifier:

$$G_{p,1} = \frac{P_{l,1}}{P_{in,1}} \tag{2.7}$$

The available power gain is defined as a ratio of the power available from the amplifier to the power available from the source:

$$G_{a,1} = \frac{P_{ava,1}}{P_{avs,1}} \tag{2.8}$$

2.1.3 Efficiency

Efficiency is a crucial parameter for RF power amplifiers especially in the battery-powered portable or mobile equipment where the input power is limited. It is also important for high-power equipment where the cost of the electric power over the lifetime of the equipment and the cost of the cooling systems can be significant compared to the purchase price of the equipment [Albulet 01]. The efficiency has several definitions: efficiency, the power added efficiency, the overall efficiency, and the long-term mean efficiency.

The efficiency is defined as:

$$\eta = \frac{P_{l,1}}{P_{DC}} \tag{2.9}$$

The long-term mean efficiency is defined as:

$$\bar{\eta} = \frac{\int_{-\infty}^{\infty} P_{l,1} \cdot g(P_{l,1}) dP_{l,1}}{\int_{-\infty}^{\infty} P_{DC}(P_{l,1}) \cdot g(P_{l,1}) dP_{l,1}} \tag{2.10}$$

where $g(P_{l,1})$ is the probability that the amplifier will have a power delivered to the load $P_{l,1}$, and $P_{DC}(P_{l,1})$ is the dc power consumption at the power delivered to the load $P_{l,1}$ [Zhang 03].

The efficiency does not take into account the required drive power, which may be quite substantial in a power amplifier. In general, RF power amplifiers designed for high efficiency tend to achieve a low power gain which is a disadvantage for the overall power budget. The power added efficiency takes the above into account and is given as:

$$PAE = \frac{P_{l,1} - P_{in,1}}{P_{DC}} = \frac{P_{l,1} - \frac{P_{l,1}}{G_{p,1}}}{P_{DC}} \tag{2.11}$$

The overall efficiency is an alternative definition of power added efficiency that takes into account the drive power and is defined as:

$$\eta_{overall} = \frac{P_{l,1}}{P_{DC} + P_{in,1}} = \frac{P_{l,1}}{P_{DC} + \frac{P_{l,1}}{G_{p,1}}} \tag{2.12}$$

2.1.4 Bandwidth

The typical frequency response of the power amplifier is shown in Fig. 2.2. The power gain can be shown instead of the output power. The output power and the

power added efficiency are shown versus frequency. This amplifier has a maximum of 28 dBm at the 2.44 GHz. To compare the frequency response of different power amplifiers, the bandwidth can be used. This example shows a commonly used 3 dB bandwidth that equals to 0.33 GHz.

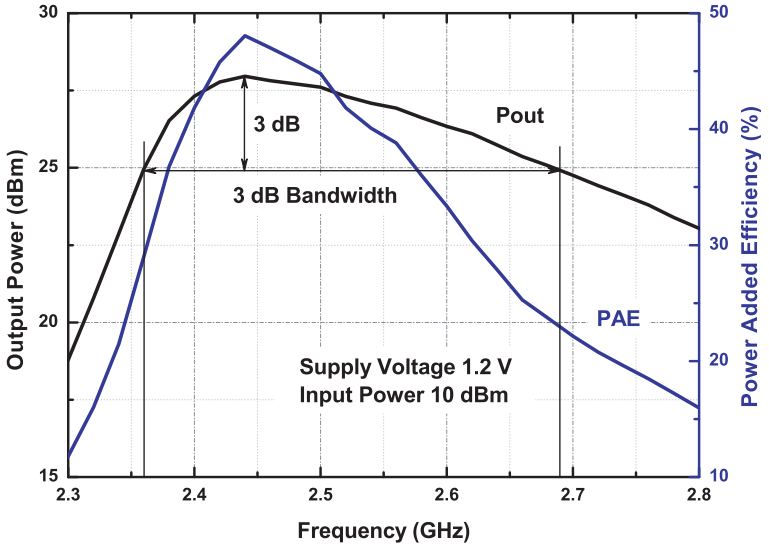


Figure 2.2: Measured frequency response of the 2 GHz band CMOS power amplifier [Vasylyev 04], showing 3 dB bandwidth definition.

2.1.5 Nonlinearity

While many analog and RF circuits can be approximated with a linear model to obtain their response to small signals, nonlinearities often lead to interesting and important phenomena [Razavi 98]. To discover it, the circuit response is approximated by the first three terms of Taylor series as:

$$y(t) \approx a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) \tag{2.13}$$

Harmonics

If a sinusoid is applied to a nonlinear system, the output generally exhibits frequency components that are integer multiples of the input frequency. In (2.13), if $x(t) = A\cos\omega t$, then

$$y(t) = a_1 A\cos\omega t + a_2 A^2\cos^2\omega t + a_3 A^3\cos^3\omega t \tag{2.14}$$

$$= a_1 A\cos\omega t + \frac{a_2 A^2}{2}(1+\cos 2\omega t) + \frac{a_3 A^3}{4}(3\cos\omega t + \cos 3\omega t) \tag{2.15}$$

$$= \frac{a_2 A^2}{2} + (a_1 A + \frac{3a_3 A^3}{4}) \cos \omega t + \frac{a_2 A^2}{2} \cos 2\omega t + \frac{a_3 A^3}{4} \cos 3\omega t \qquad (2.16)$$

In (2.16), the term with the input frequency is called the "fundamental" and the higher-order terms the "harmonics."

The next observations are made:

- Harmonics as well as dc component which are resulted from a_j with even j vanish if the system has odd symmetry (e.g. differential amplifier shown in Fig. 2.3).
- The amplitude of the n^{th} harmonic consists of a term proportional to A^n and other terms proportional to higher powers of A which can be neglected for the small A, therefore the n^{th} harmonic grows approximately in proportion to A^n for the small values of A (see Fig. 2.4).

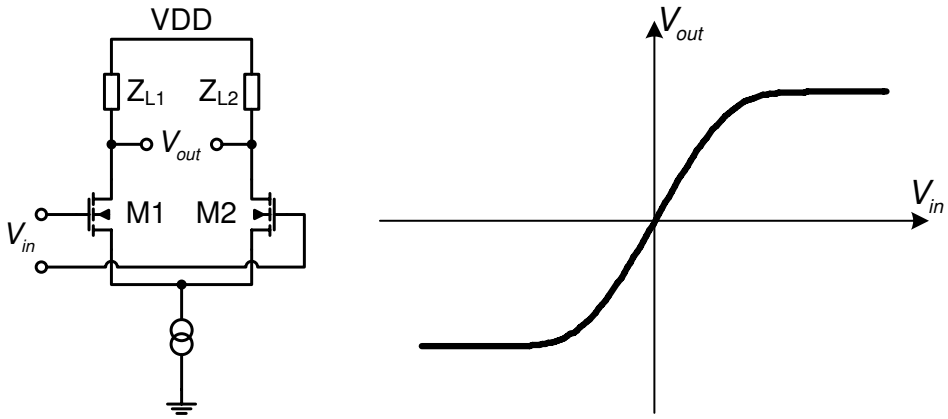


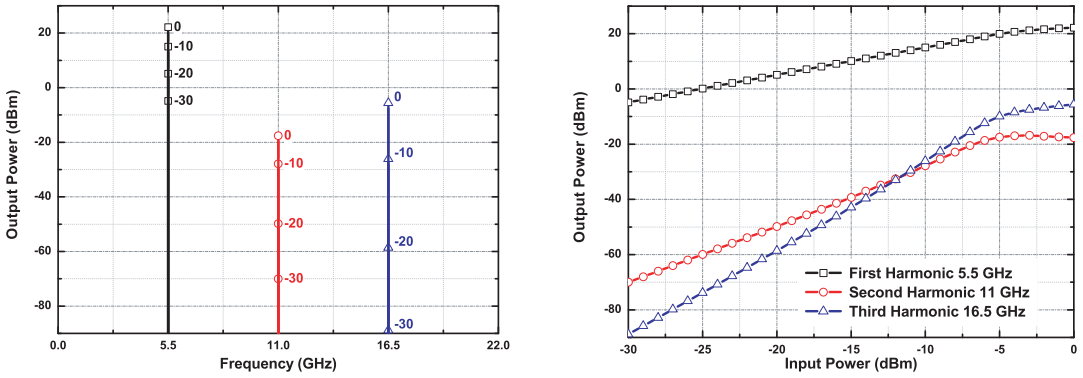
Figure 2.3: Odd symmetrical amplifier: (a) CMOS differential pair; (b) Transfer characteristic.

Gain Compression

The small-signal gain of a circuit is usually obtained with the assumption that harmonics are negligible. For example, if in (2.16), $a_1 A$ is much greater than all the other factors that contain A, then the small signal gain is equal to a_1.

However, as the signal amplitude increases, the gain begins to vary. In fact nonlinearity can be viewed as variation of the small-signal gain with the input level. This is evident from the term $3a_3 A^3/4$ added to $a_1 A$ in (2.16).

In most circuits of interest, the output is a "compressive" or "saturating" function of the input; that is, the gain approaches zero for sufficiently high input levels.



(a) (b)

Figure 2.4: Typical output spectrum of the power amplifier with a single tone at the input (Three first harmonics are shown): (a) Frequency domain; (b) Power transfer characteristic.

In (2.16) this occurs if $a_3 < 0$. Written as $a_1 + 3a_3A_3/4$, the gain is therefore a decreasing function of A. In RF circuits, this effect is quantified by the "1-dB compression point," defined as the input signal level that causes the small-signal gain to drop by 1 dB.

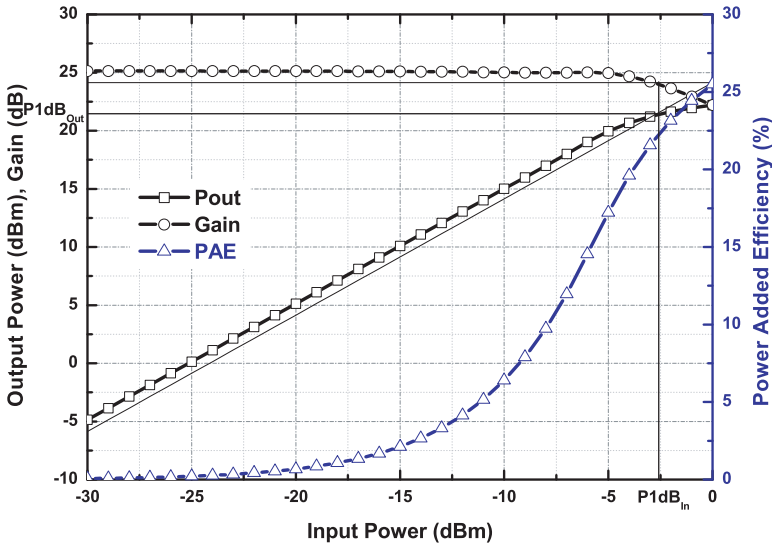


Figure 2.5: Single tone power transfer characteristic, showing graphical definition of the "1-dB compression point".

Intermodulation

While harmonic distortion is often used to describe nonlinearities of analog circuits, certain cases required other measures of nonlinear behaviour. For example, suppose the nonlinearity of a narrow band power amplifier is to be evaluated. The narrow band causes its harmonics to fall out-of the passband, and then the output distortion appears quite small even if the power amplifier introduces substantial nonlinearity. Thus, another type of test is required here. Commonly used is the "intermodulation distortion" in a "two-tone" test.

When two signals with different frequencies are applied to a nonlinear system, the output in general, exhibits some components that are not harmonics of the input frequencies and are called intermodulation (IM). This phenomenon arises from "mixing" (multiplication) of the two signals when their sum is raised to a power greater than unity. To understand how (2.13) leads to intermodulation, assume $x(t) = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t$. Thus,

$$\begin{aligned} y(t) &= a_1(A_1 \cos \omega_1 t + A_2 \cos \omega_2 t) \\ &+ a_2(A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^2 + a_3(A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^3 \end{aligned} \quad (2.17)$$

Expanding the terms in (2.17) and discarding dc terms and harmonics, we obtain the following intermodulation products:

$$\omega = \omega_1 \pm \omega_2 : a_2 A_1 A_2 \cos(\omega_1 + \omega_2)t + a_2 A_1 A_2 \cos(\omega_1 - \omega_2)t \quad (2.18)$$

$$\omega = 2\omega_1 \pm \omega_2 : \frac{3a_3 A_1^2 A_2}{4} \cos(2\omega_1 + \omega_2)t + \frac{3a_3 A_1^2 A_2}{4} \cos(2\omega_1 + \omega_2)t \quad (2.19)$$

$$\omega = 2\omega_2 \pm \omega_1 : \frac{3a_3 A_2^2 A_1}{4} \cos(2\omega_2 + \omega_1)t + \frac{3a_3 A_2^2 A_1}{4} \cos(2\omega_2 + \omega_1)t \quad (2.20)$$

and these fundamental components
$\omega = \omega_1, \omega_2 :$

$$(a_1 A_1 + \frac{3}{4} a_3 A_1^3 + \frac{3}{2} a_3 A_1 A_2^2) \cos \omega_1 t + (a_1 A_2 + \frac{3}{4} a_3 A_2^3 + \frac{3}{2} a_3 A_2 A_1^2) \cos \omega_2 t \quad (2.21)$$

The third-order IM products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are illustrated in Fig. 2.6. The key point here is that if the difference between ω_1 and ω_2 is small and they are in the band of the amplifier then the components at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$

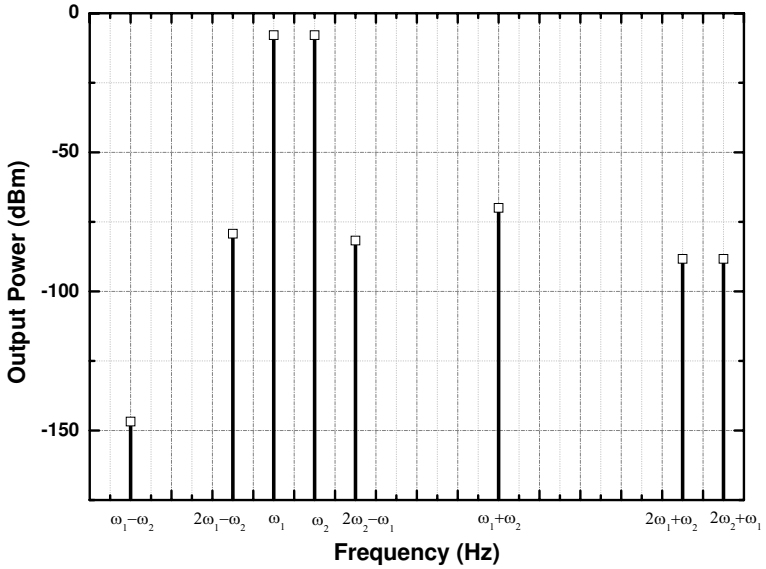


Figure 2.6: Output spectrum of two-tone analysis, showing typical intermodulation products of the power amplifier.

appear in the vicinity of ω_1 and ω_2, thus distorting the useful signal. In a typical two-tone test, $A_1 = A_2 = A$, and the ratio of the amplitude of the output third-order products to $a_1 A$ defines the IM distortion. For example, if $a_1 A = 1$ V_{pp}, and $3a_3 A_3/4 = 10$ mV_{pp}, then IM components are at -40 dBc, where the letter "c" means "with respect to the carrier."

The corruption of signals due to third-order intermodulation of two nearby interferers is so common and critical that a performance metric has been defined to characterize this behaviour. Called the "third intercept point" (IP_3), this parameter is measured by a two-tone test in which A is chosen to be sufficiently small so that higher-order nonlinear terms are negligible and the gain is relatively constant and equal to a_1. From (2.18), (2.19), and (2.20), with increasing A, the fundamentals increase in proportion to A, whereas the third-order IM products increase in proportion to A^3. The third-order intercept point is defined to be at the interception of the two lines. The horizontal coordinate of this point is called the input IP_3 (IIP_3), and the vertical coordinate is called the output IP_3 (OIP_3) (see Fig. 2.7).

Also, OIP for any intermodulation product can be determine by:

$$OIP_n = \frac{nP_A - P_{IM}}{n-1} \tag{2.22}$$

where n is a number of IM product, P_A and P_{IM} are fundamental and intermodulation product power respectively for the same input power.

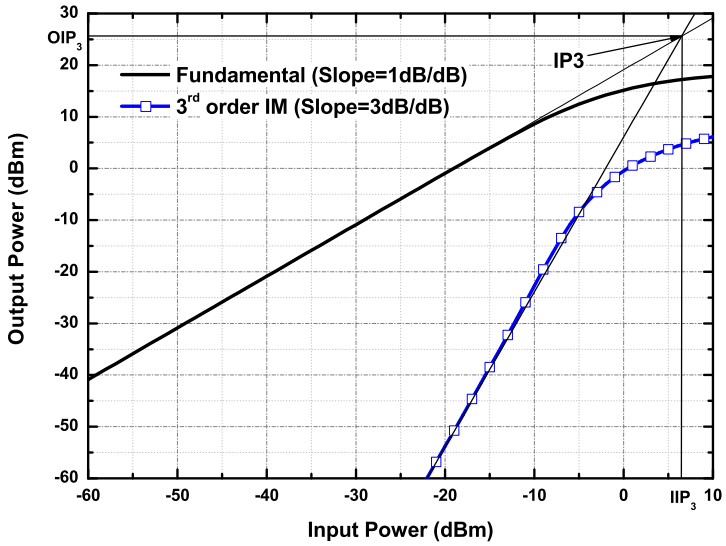


Figure 2.7: Two-tone power transfer characteristic, showing graphical definition of the third-order intercept point.

2.1.6 Error Vector Magnitude and Power Complementary Cumulative Distribution Function (OFDM Modulation)

Error vector magnitude (EVM) measurement can provide a great deal of insight into the performance of digitally modulated signals. With proper use, EVM and related measurements can pinpoint exactly the type of degradations present in a signal and can even help identify their sources [Agilent 00,b], [Agilent 04].

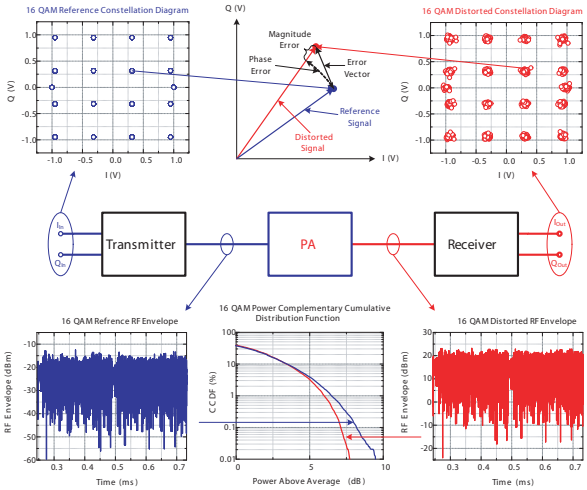


Figure 2.8: The effect of the power amplifier non-linearity on the performance of OFDM signal (WLAN 802.11a, OFDM, 52 subcarriers, 16QAM, 36 Mbps).

The EVM measurement is a modulation quality metric, widely used in digital RF communications systems, especially emerging the third generation (3G) and wireless local area networks. It is essentially a measure of the accuracy of the modulation of the transmitted waveform [Zhang 03].

Let $Z(k)$ denote the actual complex vectors (I and Q) produced by observing the real transmitter through an ideal receiver filter at instants k, one symbol period apart. Let $S(k)$ denote the ideal reference symbol. Then, $Z(k)$ is defined as:

$$Z(k) = [C_0 + C_1 S(k) + E(k)]W^k, 0 \leq k \leq N-1 \tag{2.23}$$

where N is number of symbols within burst to be measured, $W = \exp^{Dr+jDa}$ accounts for both a frequency offset (Da radians per symbol phase rotation) and an amplitude change rate (Dr nepers per symbol), C_0 is a complex constant origin offset, C_1 is a complex constant representing the arbitrary phase and output power of the amplifier, and $E(k)$ is the residual vector error on sample $S(k)$.

The sum square error vector is defined as:

$$\sum_{k=0}^{N-1} \mid E(k)|^2 = \sum_{k=0}^{N-1} \left| \frac{[Z(k)W^{-k} - C_0]}{C_1} - S(k) \right|^2 \tag{2.24}$$

where C_0, C_1, and W are chosen such as to minimize the above expression.

$EVM(rms)$ is defined to be the rms value of $|E(k)|$ normalized by the rms value of $|S(k)|$. Therefore,

$$EVM(rms) = \frac{\sqrt{\frac{1}{N}\sum_{k=0}^{N-1} \mid E(k)|^2}}{\sqrt{\frac{1}{N}\sum_{k=0}^{N-1} \mid S(k)|^2}} = \frac{\sqrt{\sum_{k=0}^{N-1} \mid E(k)|^2}}{\sqrt{\sum_{k=0}^{N-1} \mid S(k)|^2}} \tag{2.25}$$

The symbol EVM at symbol k is defined as:

$$EVM(k) = \frac{|E(k)|}{\sqrt{\frac{1}{N}\sum_{k=0}^{N-1} \mid S(k)|^2}} \tag{2.26}$$

which is the vector error magnitude at symbol k normalized by the rms value of $|S(k)|$.

Power Complementary Cumulative Distribution Function (CCDF) curves provide critical information about the signals encountered in 3G systems. These curves also provide the peak-to-average power data needed by component designers. CCDF curve shows how much time the signal spends at or above a given power level. The power level is expressed in dB relative to the average power. The percentage of time the signal spends at or above each line defines the probability for that particular power level. A CCDF curve is a plot of relative power levels versus probability and is defined as:

$$CCDF(x) = 1 - \int_{-\infty}^{x} g(P)dP \tag{2.27}$$

where $g(P)$ is the probability density function (PDF) given by the modulation scheme, hence by the probability of the symbols, the integral of the PDF is the Cumulative Distribution Function (CDF) [Agilent 00,a].

2.1.7 Adjacent Channel Power Ratio

Adjacent channel power ratio (ACPR) is a measure of the degree of signal spreading into adjacent channels, caused by nonlinearities in the power amplifier. It is defined as the power contained in a defined bandwidth (B_{n-1} or B_{n+1}) at a defined offset (f_o) from the channel center frequency (f_c), divided by the power in a defined bandwidth (B_n) placed around the channel center frequency. The bandwidths need not be the same (and indeed are not for many current standards). The concept is illustrated in Fig. 2.9 [Kenington 02].

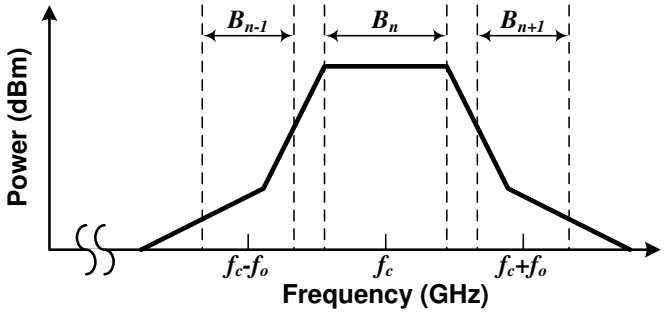


Figure 2.9: Adjacent channel power ratio.

2.1.8 Ruggedness

Power amplifiers in a mobile environment must be able to handle miss-match conditions at the antenna interface (values are system dependent):

- Survive at the VSWR ≥ 10.
- Do not show performance degradation after stress at the normal conditions.
- Preserving a high PAE and output power at the VSWR ≤ 2.5.

The measurement setup for mismatch load operation is shown in Fig. 2.10. It consists of a signal generator, a power supply, a power amplifier under test, coupler (20 dB), spectrum analyzer, variable attenuator ($0 \div 20$ dB), and a sliding short.

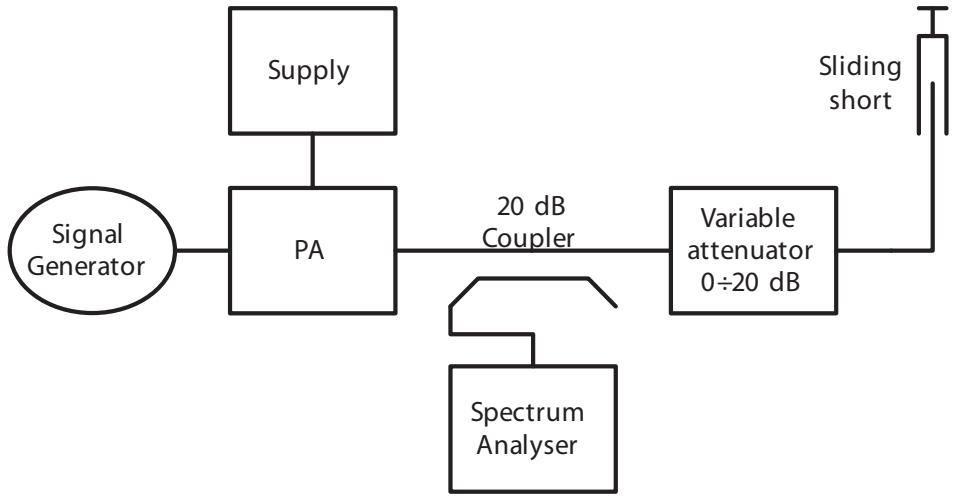


Figure 2.10: Measurement setup to operate a power amplifier under the load mismatches.

The sliding short together with the attenuator provide a variable load to the PA thereby emulating a mismatched antenna (programmable delay line can be used as the sliding short). The directional coupler couples -20 dB of the output power from the PA into the spectrum analyzer. Thus the harmonics and spurs can be measured under different mismatch conditions.

2.2 Basic Tuned Amplifier Classes

The power amplifiers are divided in two main classes "linear" and "nonlinear" or switched mode. "Linear" power amplifiers operate in the Forward Active (bipolar) and Saturation (MOS) regions; and "nonlinear" one operate by switching between Cutoff and Saturation (bipolar) or Triode (MOS) regions in accordance with Table 2.1.

Table 2.1: Operating regions of npn bipolar and n-channel MOS transistors [Gray 01].

npn Bipolar Transistor			**n-channel MOS Transistor**		
Region	$\mathbf{V_{BE}}$	$\mathbf{V_{BC}}$	**Region**	$\mathbf{V_{GS}}$	$\mathbf{V_{GD}}$
Cutoff	$< V_{BE(on)}$	$< V_{BC(on)}$	**Cutoff**	$< V_t$	$< V_t$
Forward Active	$\geq V_{BE(on)}$	$< V_{BC(on)}$	**Saturation(Active)**	$\geq V_t$	$< V_t$
Reverse Active	$< V_{BE(on)}$	$\geq V_{BC(on)}$	**Saturation(Active)**	$< V_t$	$\geq V_t$
Saturation	$\geq V_{BE(on)}$	$\geq V_{BC(on)}$	**Triode**	$\geq V_t$	$\geq V_t$

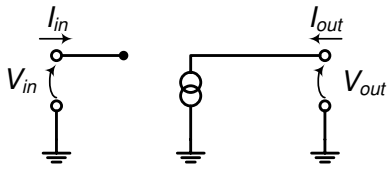


Figure 2.11: Simplified transistor model in the common emitter (source) configuration.

Fig. 2.11 shows the simplified transistor model in a common emitter (source) configuration. The transfer characteristic and output characteristic family are shown in Fig. 2.12. As can be seen from Fig. 2.12, the model has zero turn on voltage ($V_{BE(on)} = 0$ for bipolar and $V_t = 0$ for MOS transistor), the linear transconductance (the output current I_{out} linearly depends on the input voltage V_{in}) in the range ($0 < V_{in} < V_{in\_max}$) when ($V_{out} > 0$). It changes linearly from 0 and reaches its maximum (I_{out_max}) at V_{in_max}. The model has a strong saturation for $V_{in} > V_{in\_max}$.

Fig. 2.13 shows a simplified transistor model where transistor is treated as an ideal switch. That means that transistor just has two states one is on (short circuit) and second is off (open circuit); and an instantaneous transition time between them. The state of the switch or its impedance is controlled by the input voltage V_{in} and can be expressed as:

$$R_{on} = \begin{cases} 0 & V_{in} \geq V_{BE(on)} \\ \infty & V_{in} < V_{BE(on)} \end{cases} \tag{2.28}$$

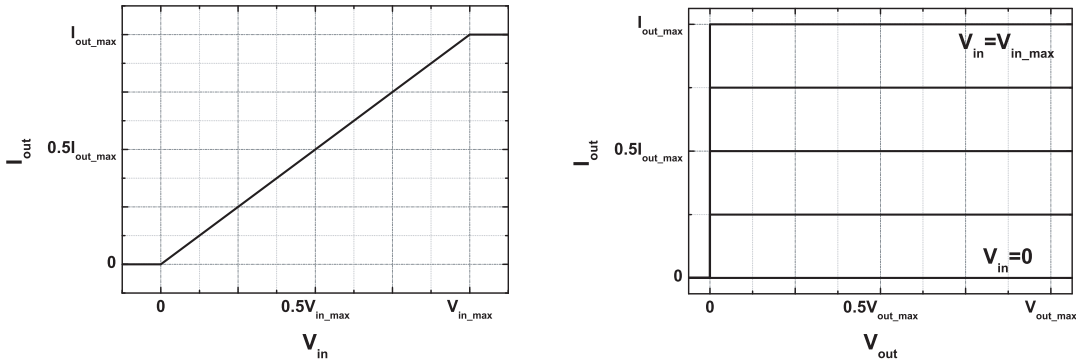


Figure 2.12: The common source (emitter) configuration: (a) Transfer characteristic; (b) Output characteristic family.

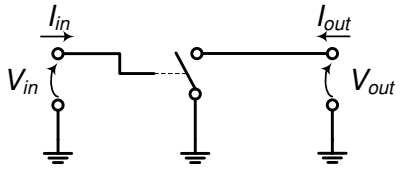


Figure 2.13: Simplified transistor model for switched mode power amplifiers.

2.2.1 Linear Tuned Power Amplifiers

There are exists three main linear power amplifier classes A, AB, B and C. Let's consider the simplified circuit diagram in Fig. 2.14. The current source of the transistor sees the load impendence R_l at a fundamental frequency and a short circuit at higher harmonics.

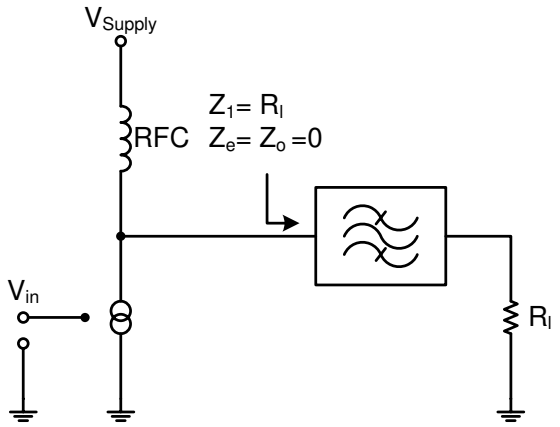


Figure 2.14: Simplified circuit diagram of the linear tuned power amplifier.

Fig. 2.15 shows the input voltage and output current waveforms. The input

voltage is a cosines with a defined quiescent voltage, amplitude that equals $V_{in\_max} - V_{In\_Q}$ and peak-to-peak voltage that is greater or equal to V_{in_max}.

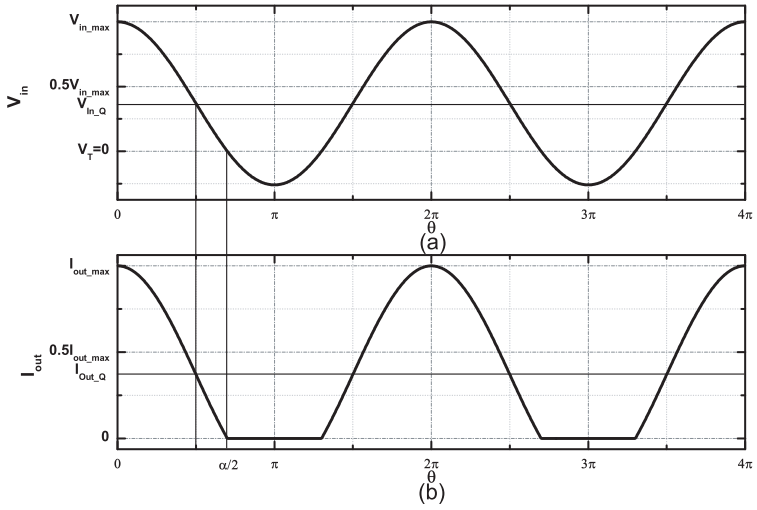


Figure 2.15: Reduced conduction angle waveforms, showing influence of the operating point at the output current waveform: (a) Input voltage; (b) Output current.

The input voltage waveform V_{in} determines the output current waveform that can be written as:

$$I_{out}(\theta) = \begin{cases} I_{Out\_Q} + I_{Amp}\cos(\theta) & -\alpha/2 < \theta < \alpha/2 \\ 0 & -\pi < \theta < -\alpha/2; \alpha/2 < \theta < \pi \end{cases} \tag{2.29}$$

where α is a conduction angle that indicates the proportion of the working cycle for which the output current exists, I_{Out_Q} is an output quiescent current, and I_{Amp} is an output amplitude.

The output current waveform parameters in (2.28) such as I_{Out_Q} and I_{Amp} can be expressed trough α and I_{max} by setting (2.28) equal to zero at $\theta = \alpha/2$ and to I_{max} at $\theta = 0$, which produce:

$$\begin{cases} 0 = I_{Out\_Q} + I_{Amp}\cos(\alpha/2) \\ I_{out\_max} = I_{Out\_Q} + I_{Amp}\cos(0) \end{cases} \tag{2.30}$$

Rearrangement of (2.30) produces:

$$\begin{cases} I_{Amp} = \frac{I_{Out\_max}}{1-\cos(\alpha/2)} \\ I_{Out\_Q} = -\frac{I_{Out\_max}\cos(\alpha/2)}{1-\cos(\alpha/2)} \end{cases} \tag{2.31}$$

Substitution of I_{Amp} and I_{Out_Q} in (2.28) then produces:

$$I_{out}(\theta) = \begin{cases} \frac{I_{Out\_max}}{1-\cos(\alpha/2)}[\cos(\theta) - \cos(\alpha/2)] & -\alpha/2 < \theta < \alpha/2 \\ 0 & -\pi < \theta < -\alpha/2; \alpha/2 < \theta < \pi \end{cases} \tag{2.32}$$

Applying of the forward Fourier transformation for (2.32) gives the dc and amplitude of harmonic components for the output current waveform:

$$I_{dc} = \frac{1}{2\pi} \int_{-\alpha/2}^{\alpha/2} \frac{I_{Out\_max}}{1-\cos(\alpha/2)}[\cos(\theta) - \cos(\alpha/2)]d\theta \tag{2.33}$$

and

$$I_n = \frac{1}{\pi} \int_{-\alpha/2}^{\alpha/2} \frac{I_{Out\_max}}{1-\cos(\alpha/2)}[\cos(\theta) - \cos(\alpha/2)]\cos(n\theta)d\theta \tag{2.34}$$

where n is a harmonic number.

Solving of (2.33) yields:

$$I_{dc} = \frac{I_{out\_max}}{2\pi} \frac{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}{1-\cos(\alpha/2)} \tag{2.35}$$

and (2.34) for the first harmonic yields:

$$I_1 = \frac{I_{out\_max}}{2\pi} \frac{\alpha - \sin(\alpha)}{1-\cos(\alpha/2)} \tag{2.36}$$

The output voltage consists of the dc voltage V_{dc} and the first harmonic. The amplitude of the first harmonic (V_1) equals to V_{dc} to get the highest efficiency and output power for a certain conduction angle:

$$\eta = \frac{P_{l,1}}{P_{dc}} = \frac{V_1 I_1}{2V_{dc}I_{dc}} = \frac{V_{dc}}{2V_{dc}} \frac{I_1}{I_{dc}} = \frac{I_1}{2I_{dc}} \tag{2.37}$$

Substitution of I_1 and I_{dc} in (2.37) then produces:

$$\eta = \frac{\alpha - \sin(\alpha)}{2(2\sin(\alpha/2) - \alpha\cos(\alpha/2))} \tag{2.38}$$

The load impedance, obtained by dividing V_1 and I_1, equals:

$$R_l = \frac{V_1}{I_1} = 2\pi \frac{V_{dc}}{I_{out\_max}} \frac{1-\cos(\alpha/2)}{\alpha - \sin(\alpha)} \tag{2.39}$$

The classification of the "linear" power amplifier in accordance with the conduction angle is shown in Table 2.2. The table also indicates operating point conditions.

Table 2.2: Amplifier classes in accordance with conduction angle.

Class	**Input quiescent voltage**	**Output quiescent current**	**Conduction angle**
A	$0.5 \cdot V_{In\_max}$	$0.5 \cdot I_{OUT\_max}$	2π
AB	$(0..0.5) \cdot V_{In\_max}$	$(0..0.5) \cdot I_{OUT\_max}$	2π .. π
B	0	0	π
C	< 0	0	π .. 0

An input voltage, output voltage and output current wave forms and load lines for different power amplifier classes are shown in Fig. 2.16.

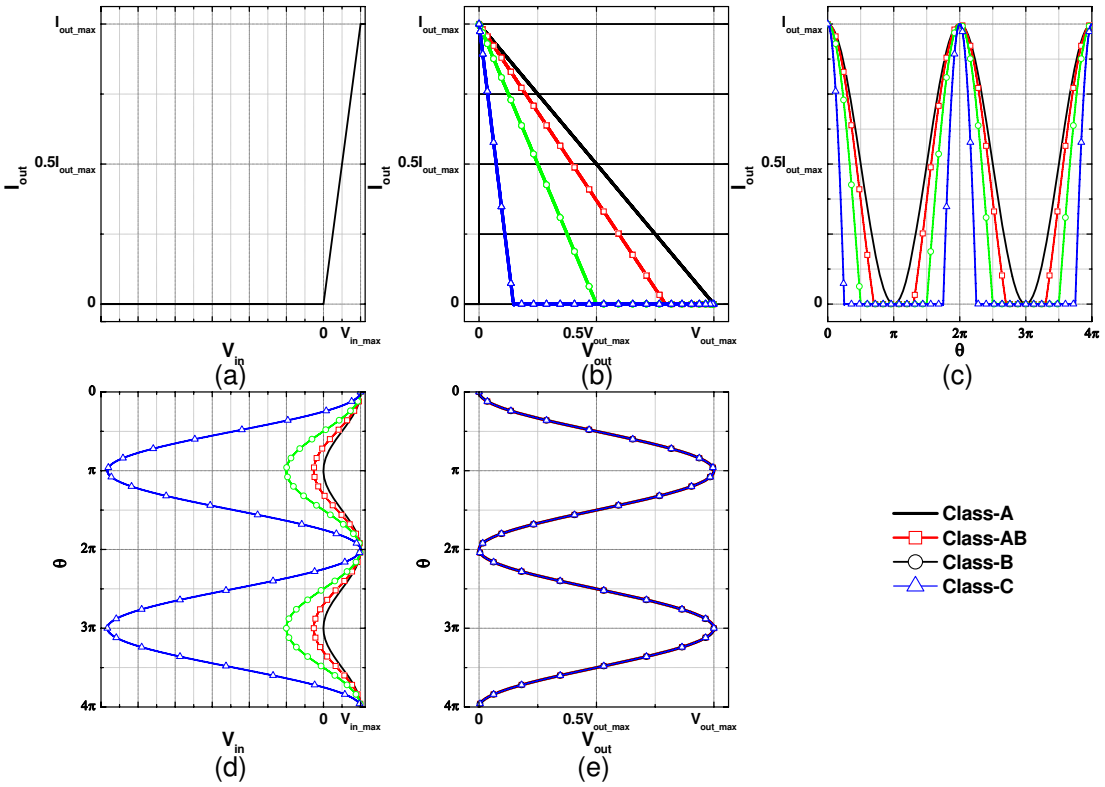


Figure 2.16: Wave forms and load lines of the linear tuned power amplifier classes (black - Class-A, red - Class-AB, green - Class-B, blue - Class-C): (a) Transfer characteristic; (b) Output characteristics with load lines; (c) Output current waveforms; (d) Input voltage waveforms; (e) Output voltage waveforms.

Harmonic content of the output current of the linear power amplifiers are presented in Fig. 2.17. THe following conclusions are made after the analysis of Fig. 2.17:

- The highest dc current is achieved when the conduction angle α equals 2π and it converges to zero when conduction angle reaches zero.
- Class-A has just a fundamental content in the output current.
- Class-AB exhibits the highest magnitude of the fundamental harmonic.
- Class-B achieves the same magnitude of the fundamental harmonic as Class-A with odd harmonics equal to zero.
- Class-C has the lowest dc current but also the lowest magnitude of a fundamental harmonic which converges to zero when conduction angle reaches zero.

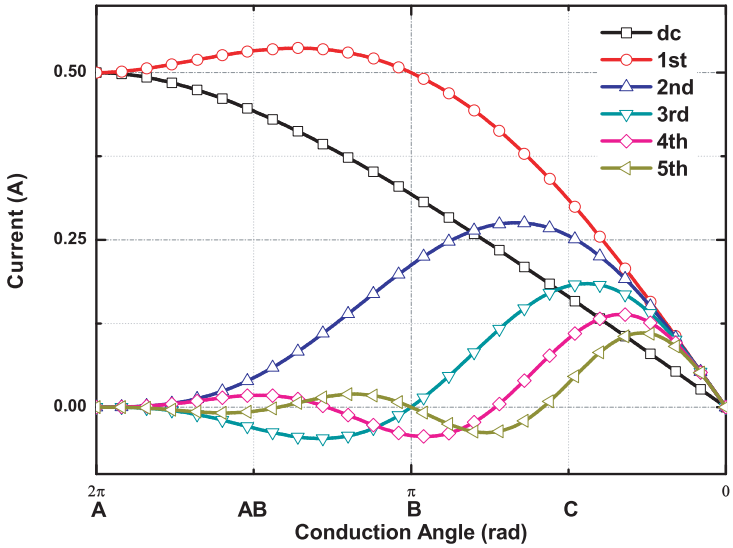


Figure 2.17: Fourier analysis versus conduction angle.

The output power of the fundamental harmonic and efficiency (2.38) versus conduction angle, when output voltage waveforms have equal peak voltage, is presented in Fig. 2.18. Next, conclusions can be made after analysis of Fig. 2.18:

- Class-A has the lowest efficiency.
- Class-AB has the highest output power.
- Class-B has the same output power as Class-A but higher efficiency.
- Class-C has the highest efficiency but the lowest output power.

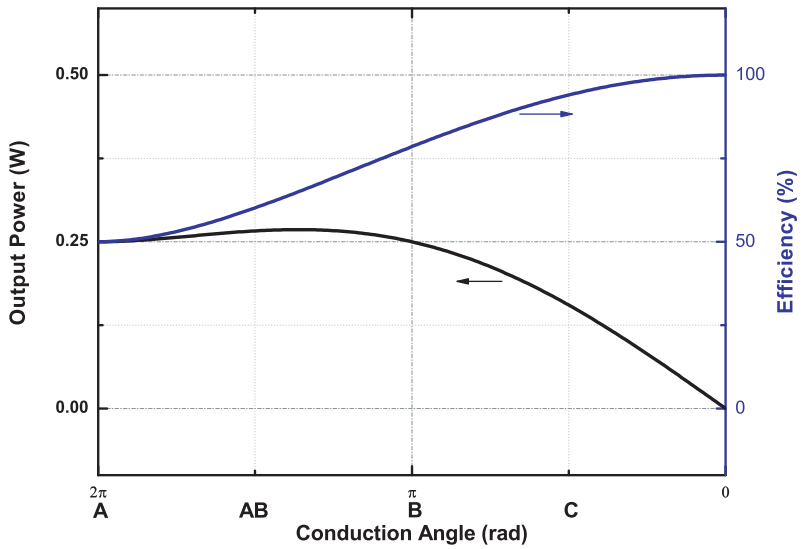


Figure 2.18: Output power and efficiency versus conduction angle.

2.2.2 Switched Mode Tuned Power Amplifiers

Class-E Tuned Power Amplifier

The Class-E power amplifier was introduced by Sokals in 1975 [Sokal 75]. The definition of Class E operation by Sokals indicates the next conditions for voltage across a transistor [Sokal 75]:

- The rise in voltage across the transistor at turn-off should be delayed till transistor is off.
- The voltage across the transistor should be brought back to zero at the time of transistor turn-on.
- The slope of the voltage across the transistor should be zero at the time of turn-on.

An amplifier that contains a switch and a load network and meets the conditions described above is called "optimum" Class-E and the one which does not meet these conditions is called "suboptimum" Class-E [Raab 77].

Fig. 2.19 shows a basic circuit of Class-E power amplifier. The circuit consists of an RF choke (RFC), transistor as a Switch (S), shunt capacitor (C), serial resonant circuit L_1C_1), and load (R_l). Fig. 2.20 represents an equivalent circuit proposed by Raab [Raab 77] where the resonant circuit (L_1C_1) was split in to the serial resonant contour (L_sC_s) with resonance at the operating frequency with an additional reactance (X). The serial resonant contour (L_sC_s) has a high enough quality factor that hinders the higher harmonics to reach the load.

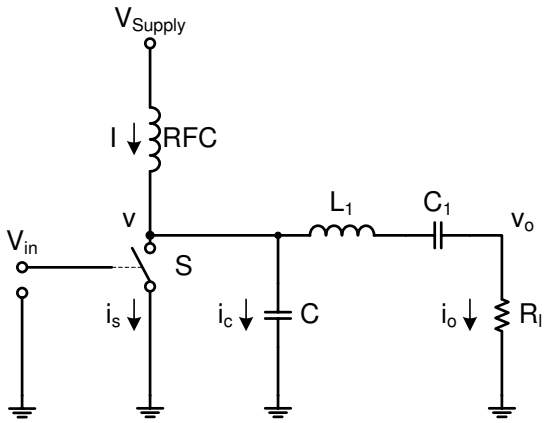


Figure 2.19: Class-E amplifier basic circuit.

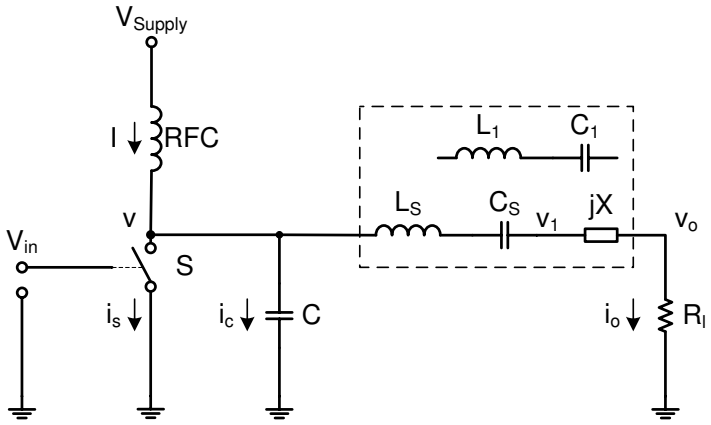


Figure 2.20: Class-E amplifier equivalent circuit.

Fig. 2.21 shows the waveforms of the "optimum" Class-E power amplifier.
The output voltage and output current are sinusoidal and expressed as:

$$v_O(\theta) = c\sin(\omega t + \varphi) = c\sin(\theta + \varphi) \tag{2.40}$$

and

$$i_O(\theta) = \frac{c}{R_l}\sin(\omega t + \varphi) = \frac{c}{R_l}\sin(\theta + \varphi) \tag{2.41}$$

where θ is an "angular time", c is an amplitude, φ is an initial phase (see Fig. 2.21), R_l is a load resistance.

Due to the high quality factor of the resonant circuit (L_sC_s) the hypothetical voltage v_1 is also a sinusoid, but has a different phase and amplitude due to the reactance (X) and equals:

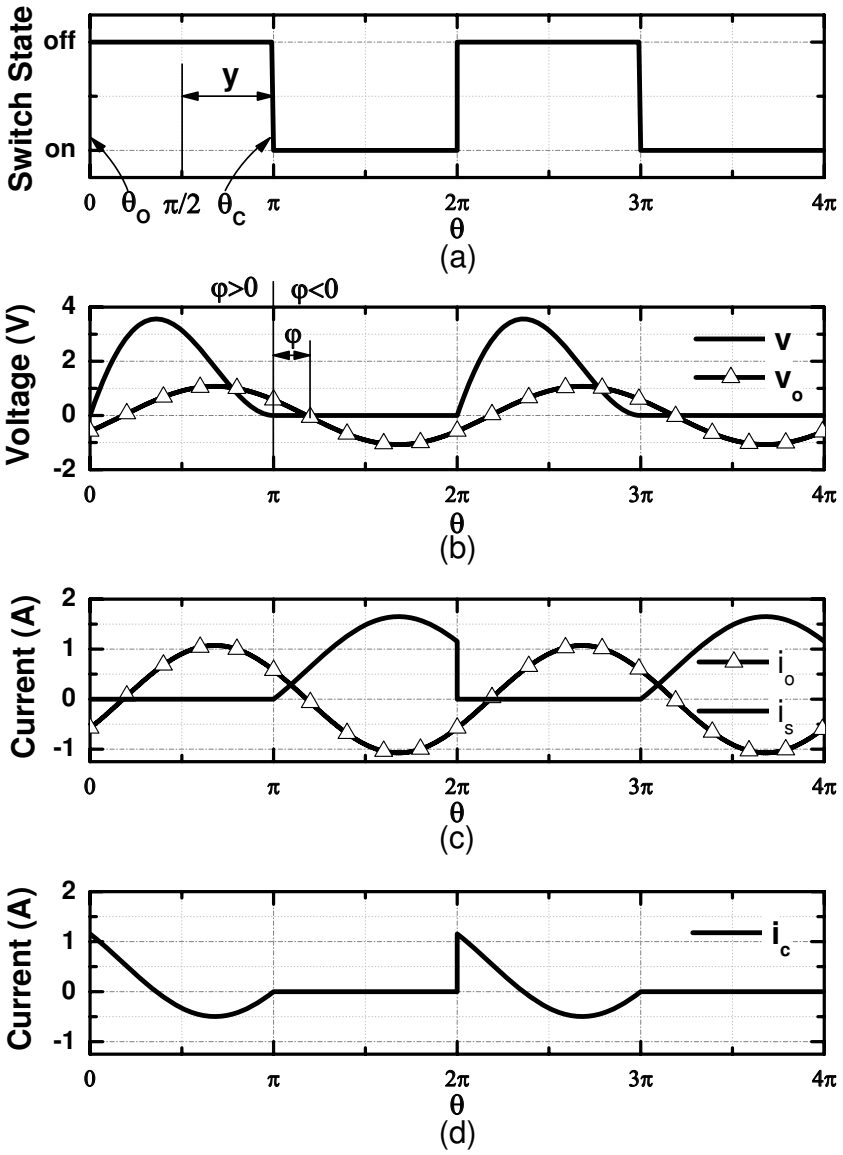


Figure 2.21: Waveforms of the "optimum" Class-E power amplifier: (a) Switch states; (b) Output voltage and voltage across the switch; (c) Output current and switch current; (d) Capacitor current.

$$v_1(\theta) = v_O(\theta) + v_X(\theta) = c\sin(\theta+\varphi) + X\frac{c}{R_l}\sin(\theta+\varphi) = c_1\sin(\theta+\varphi_1) \quad (2.42)$$

where

$$c_1 = c\sqrt{1+\frac{X^2}{R_l^2}} = c\rho \quad (2.43)$$

and

$$\varphi_1 = \varphi + \tan\left(\frac{X}{R_l}\right) = \varphi + \psi \tag{2.44}$$

The voltage across the switch (S) is produced by the charging of capacitor (C), when it's off, and equals:

$$v(\theta) = \frac{1}{\omega C}\int_{\theta_O}^{\theta} i_c(\theta)d\theta \tag{2.45}$$

where θ_O is the angular time when switch (S) opens.

The center of the off-time is arbitrarily defined as $\pi/2$ (see Fig. 2.21). The switch (S) is opened from $\theta_O = \pi/2 - y$ to $\theta_C = \pi/2 + y$. Changing capacitor current (i_c) is given by the difference between dc current (I) and output current (i_O) in (2.45), as:

$$\begin{aligned} v(\theta) &= \frac{1}{B}\int_{(\pi/2)-y}^{\theta} [I - \frac{c}{R_l}\sin(\theta+\varphi)]d\theta \\ &= \left[\frac{I}{B}\left(-\frac{\pi}{2}+y\right) + \frac{c}{BR_l}\sin(\varphi - y)\right] + \frac{I}{B}\theta + \frac{c}{BR_l}\cos(\theta+\varphi) \end{aligned} \tag{2.46}$$

where

$$B = \omega C \tag{2.47}$$

As the ideal RF choke has now dc drop, the power supply voltage (V_{Supply}) can be found as dc component of the voltage across the switch (S) by Fourier integral, that gives:

$$V_{Supply} = \frac{1}{2\pi}\int_{0}^{2\pi} v(\theta)d\theta \tag{2.48}$$

The component values (B, X) and the amplitude of the output voltage (c) in the circuit (Fig. 2.20) can be found analytically by solving (2.46) and (2.48) [Raab 77]:

$$B = \frac{2}{(1+\pi^2/4)R_l} = \frac{1}{5.4466R_l} \tag{2.49}$$

$$X = \frac{\pi}{8}\left(\frac{\pi^2}{2} - 2\right) R_l = 1.1525 R_l \tag{2.50}$$

$$c = \frac{2}{\sqrt{1 + \pi^2/4}} V_{Supply} \tag{2.51}$$

The component values in (2.49), (2.50), and (2.51) are given for a 50 % duty cycle and a zero slope of the voltage across the transistor at the turn-on time (in [Raab 77] has proved that these conditions produce the peak power-output capability of a given device and eliminates both negative voltage across the switch (S) and negative current through the switch (S) that is very useful when the ideal switch is changed by the real device.

Class-F Tuned Power Amplifier

Fig. 2.22 shows a basic circuit of Class F power amplifier. This power amplifier concept is based on the following principles:

- Fundamental harmonic of the voltage across the switch and current through the switch are 180° out-of phase.
- When the voltage across the switch adds odd harmonics to build its shape to a square wave, then the current through the switch adds even harmonics to build its shape toward a half sine wave or vice versa.
- No power is generated at the harmonics because there is either no voltage or no current at a given harmonic. Harmonic impedance is either zero or infinite.

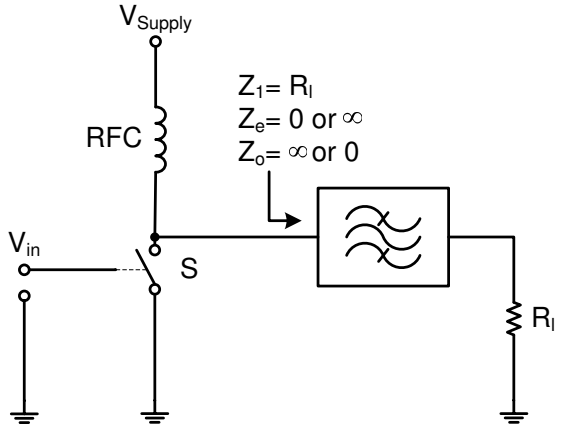


Figure 2.22: Basic circuit of Class-F power amplifier.

To find the Fourier coefficients for maximum power and efficiency (see Table 2.3 and 2.4), it is convenient to fix the fundamental harmonic amplitude at unity. The amplitude of the harmonic(s) is then adjusted to minimize the downward excursion of the waveform. Fixing the waveform minimum to zero gives the minimum supply voltage needed for full output which in turn, minimizes the dc-input power and therefore maximizes efficiency. Flattening of the waveform reduces the peak voltage and therefore maximizes the power-output capability for a given rating. Thus, maximum efficiency and maximum output power capability occur for the same waveform coefficients and are listed in Table 2.5 and 2.6 respectively, where the output power capability is obtained by dividing the output power by peak voltage and current [Raab 01].

Table 2.3: Maximum efficiency waveform coefficients for odd harmonics.

Harm.	$\mathbf{V_{max}/V_D}$	$\mathbf{V_{om}/V_D}$	$\mathbf{V_{3m}/V_{om}}$	$\mathbf{V_{5m}/V_{om}}$
$\mathbf{n = 1}$	2	1	0	0
$\mathbf{n = 3}$	2	1.1547	0.1667	0
$\mathbf{n = 5}$	2	1.05146	0	-0.0618
$\mathbf{n = 3\&5}$	2	1.2071	0.2323	0.0607
$\mathbf{n = \infty}$	2	$4/\pi = 1.273$	$4/3\pi = 0.424$	$4/5\pi = 0.255$

Table 2.4: Maximum efficiency waveform coefficients for even harmonics.

Harm.	$\mathbf{I_{max}/I_{dc}}$	$\mathbf{I_{om}/I_{dc}}$	$\mathbf{I_{2m}/I_{om}}$	$\mathbf{I_{4m}/I_{om}}$
$\mathbf{n = 1}$	2	1	0	0
$\mathbf{n = 3}$	2.9142	1.4142	0.354	0
$\mathbf{n = 5}$	2.1863	1.0824	0	-0.0957
$\mathbf{n = 3\&5}$	3	1.5	0.389	0.0556
$\mathbf{n = \infty}$	π	$\pi/2 = 1.571$	$2/3 = 0.667$	$2/15 = 0.133$

Table 2.5: Maximum efficiency of Class-F power amplifiers.

	n = 1	**n = 3**	**n = 5**	**n = ∞**
m = 1	1/2=0.5	$1/3^{1/2} = 0.5774$	0.6033	$2/\pi = 0.637$
m = 2	0.7071	0.8165	0.8532	0.9003
m = 4	0.7497	0.8656	0.9045	0.9545
m = ∞	$\pi/4 = 0.785$	0.9069	0.9477	1

Table 2.6: Maximum power-output capability of Class-F power amplifiers.

n = 1	**n = 3**	**n = 5**	**n = ∞**
1/8=0.125	$1/4/3^{1/2} = 0.1443$	0.1508	$1/2\pi = 0.159$

Fig. 2.23 shows four pairs of waveforms of an ideal Class-F power amplifier which correspond to the diagonal cells of Table 2.5.

Class-D Tuned Power Amplifier

Class-D power amplifier (see Fig. 2.24) consists of a two-pole switch (S) that defines either a rectangular voltage or rectangular current waveform at the input of a tuned circuit (L_1C_1) that includes the load (R_l). Fig. 2.25 shows the principle of work of ideal Class-D amplifier.

Fig. 2.26 shows Class-D implementation were two-pole switch is changed by two MOS transistors. The transistors are connected in such way that they work in anti-phase (when one is on, the second is off). The output tuned circuit should have high enough quality factor to suppress higher harmonics at the load.

The voltage at the two-pole switch output (v) for the 50 % duty cycle is a meander and can be described as follows:

$$v(\theta) = V_{Suppy}\left(\frac{1}{2} + \frac{1}{2}b(\theta)\right) \tag{2.52}$$

where $b(\theta)$ is given by:

$$b(\theta) = \begin{cases} +1 & sin(\theta) \geq 0 \\ -1 & sin(\theta) < 0 \end{cases} \tag{2.53}$$

Expansion of $b(\theta)$ by Fourier series gives:

$$b(\theta) = \frac{4}{\pi}\left(sin(\theta) + \frac{1}{3}sin(3\theta) + \frac{1}{5}sin(5\theta) + \cdots\right) \tag{2.54}$$

Substitution of (2.54) in (2.52) gives:

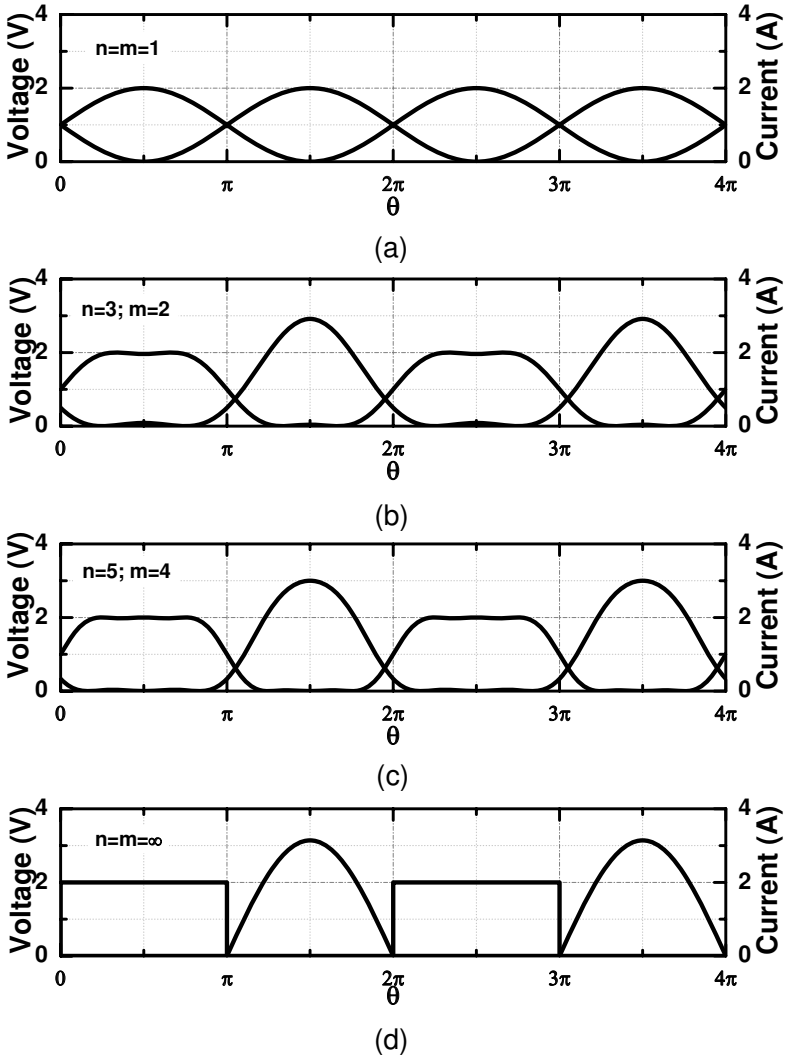


Figure 2.23: Class-F waveforms, showing the influence of the harmonic content on the shape of the waveforms: (a) Voltage and current contain just fundamental harmonics; (b) Voltage contains fundamental and third harmonic. Current contains fundamental and second harmonic; (c) Voltage contains fundamental, third and fifth harmonics. Current contains fundamental, second and fourth harmonics; (d) Voltage contains fundamental and all odd harmonics. Current contains fundamental and all even harmonics.

$$v(\theta) = V_{Supply}\left(\frac{1}{2} + \frac{2}{\pi}sin(\theta) + \frac{2}{3\pi}sin(3\theta) + \frac{2}{5\pi}sin(5\theta) + \cdots\right) \tag{2.55}$$

The output current is sinusoidal due to the tuned circuit and equals:

$$i_o(\theta) = \frac{2V_{Supply}}{\pi R_l}sin(\theta) \tag{2.56}$$

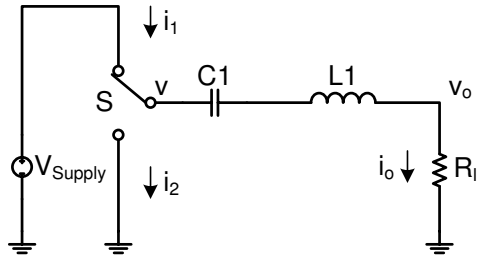


Figure 2.24: Basic circuit of Class-D power amplifier.

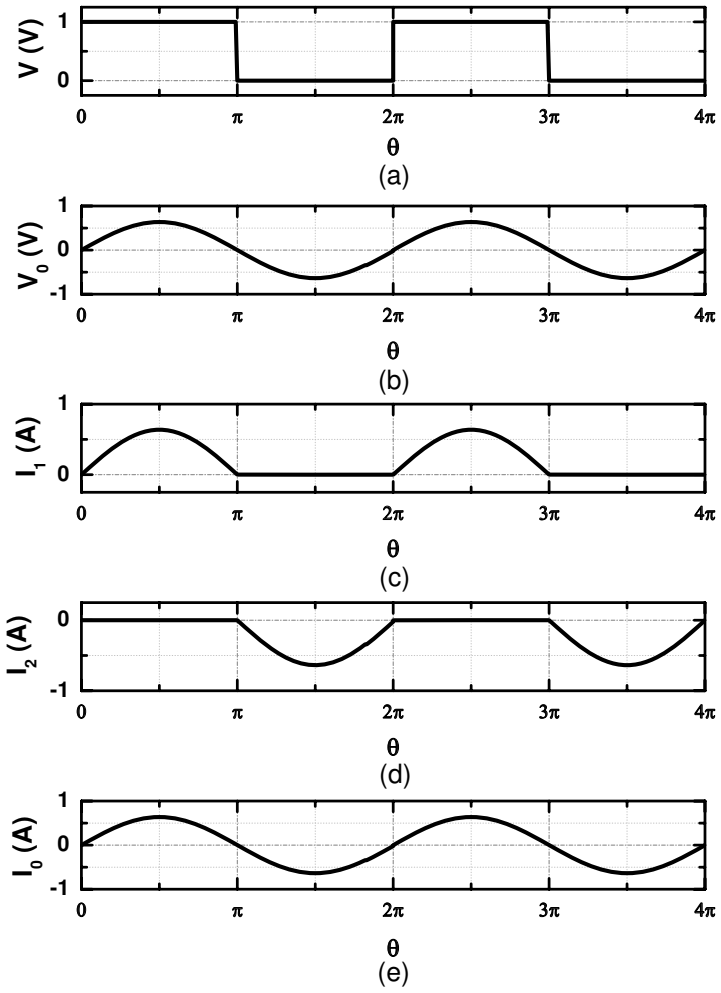


Figure 2.25: Class-D waveforms: (a) Switch output voltage; (b) Output voltage; (c) Charging current; (d) Discharging current; (e) Output current.

Multiplying (2.56) with load resistance (R_l) gives the output voltage:

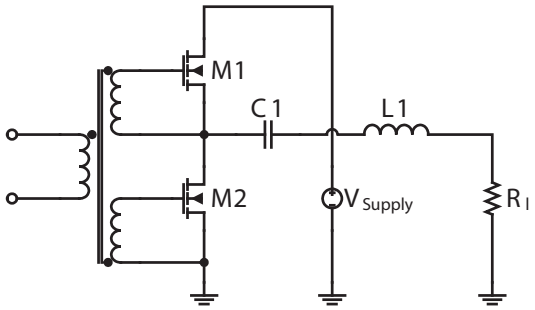


Figure 2.26: Class-D implementation.

$$v_o(\theta) = \frac{2V_{Supply}}{\pi} sin(\theta) \tag{2.57}$$

The output power is then given by:

$$P_o = \frac{1}{2}\frac{2V_{Supply}}{\pi R_l}\frac{2V_{Supply}}{\pi} = \frac{2}{\pi^2}\frac{V_{Supply}^2}{R_l} \tag{2.58}$$

The dc current is the average of the current i_1 which is acquired from half period of the output current (i_o) and equals:

$$I_{dc} = \frac{1}{2\pi}\int_0^{\pi} i_o(\theta)d\theta = \frac{1}{2\pi}\int_0^{\pi} \frac{2V_{Supply}}{\pi R_l} sin(\theta)d\theta = \frac{2}{\pi^2}\frac{V_{Supply}}{R_l} \tag{2.59}$$

The dc power consumption is given by:

$$P_{dc} = V_{Supply} I_{dc} = \frac{2}{\pi^2}\frac{V_{Supply}^2}{R_l} \tag{2.60}$$

The output power (2.58) equals the dc power consumption (2.60) that leads to an efficiency of 100 %:

$$\eta = \frac{P_o}{P_{dc}} = 1 \tag{2.61}$$

Chapter 3

Silicon Based Technologies for Power Amplifier Design

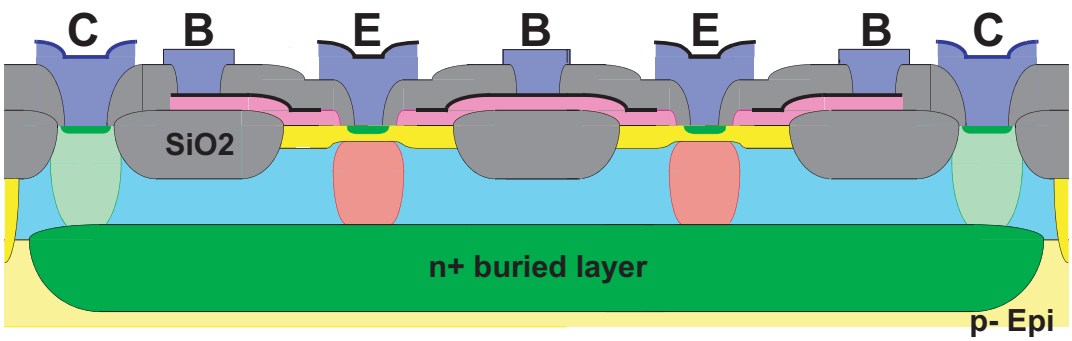
3.1 Active Components

3.1.1 Bipolar Transistors

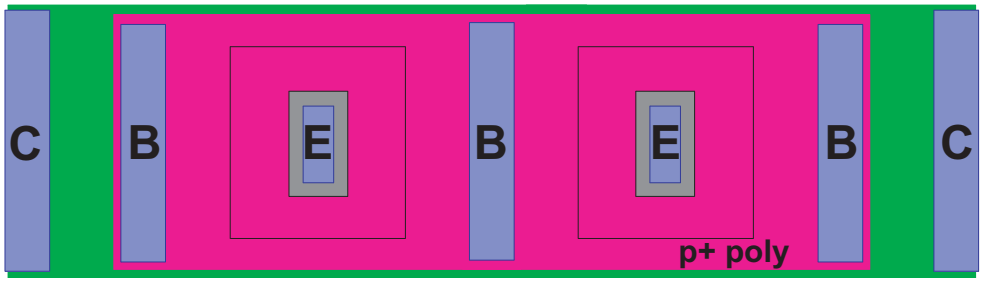
Resent modern SiGe bipolar technologies show impressive transistor characteristics: the transit frequency above 200 GHz and the maximum oscillation frequency above 300 GHz. Unfortunately, they suffer from the low breakdown voltage ($BV_{CE0} < 2\ V$) that make them not suitable for the GSM power amplifier applications with supply voltage up to 4.5 V. The used technology is developed especially for power amplifier applications and represents a trade-off between the transit frequency and breakdown voltage. As a compromise, a transit frequency of 28 GHz was adjusted which increases the breakdown voltage BV_{CE0} to 8 V. Fig. 3.1 shows the typical cross-section of the power NPN transistor.

The modern technologies as well as their applications require an accurate device modelling. The widely used Ebers-Moll or Gummel-Poon models are not able to give the required accuracy for high frequency and high current density applications. Additional external components can be added to reduce the discrepancy between the real modern devices and their models. To overcome this problem the recently developed HICUM model is used [Schroeter 05]. The main features of this model are:

- Distributed high-frequency model for the external base-collector region.
- Temperature dependence and self-heating.
- Weak avalanche breakdown at the base-collector junction.
- Bandgap difference (occurring in HBTs).



(a)



(b)

Figure 3.1: Power NPN silicon bipolar transistor with junction isolation and self-aligned base-emitter formation: (a) Schematic cross-section; (b) Layout.

Equivalent Circuit

The *HI*gh-*CU*rrent *M*odel, referred as HICUM, is a semi-physical compact bipolar transistor model. Semi-physical means that for arbitrary transistor configurations, defined by the emitter size as well as the number and location of base, emitter and collector fingers (or contacts), a complete set of model parameters can be calculated from a single set of technology specific electrical and technological data [Schroeter 05]. The large-signal HICUM/Level2 equivalent circuit is shown in Fig. 3.2.

The total transfer (collector) current is given by:

$$i_T = i_{Tf} - i_{Tr} = \frac{c_{10}}{Q_{p,T}} \exp\left(\frac{v_{B'E'}}{m_{Cf} V_T}\right) - \frac{c_{10}}{Q_{p,T}} \exp\left(\frac{v_{B'C'}}{V_T}\right) \tag{3.1}$$

where i_{Tf} and i_{Tr} are "forward" and "reverse" components of the transfer current; m_{Cf} is the non-ideality coefficient; $Q_{p,T}$ is a hole charge; c_{10} is the model parameter.

Equation (3.1) can also be written as:

$$i_T = \frac{I_S}{Q_{p,T}/Q_{p0}} \left[\exp\left(\frac{v_{B'E'}}{m_{Cf} V_T}\right) - \exp\left(\frac{v_{B'C'}}{V_T}\right)\right] \tag{3.2}$$

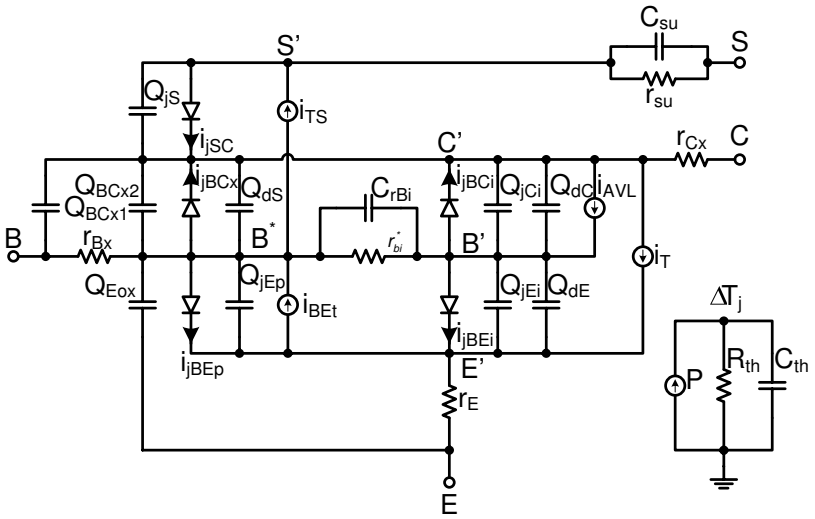


Figure 3.2: Large-signal HICUM/Level2 equivalent circuit.

where I_S is the usual collector saturation current which equals to c_{10}/Q_{p0}; Q_{p0} is the hole charge at zero bias.

The quasi-static internal base current, which represents injection across the bottom emitter area, is modelled in HICUM as:

$$i_{jBEi} = I_{BEiS}\left[\exp\left(\frac{v_{B'E'}}{m_{BEi}V_T}\right) - 1\right] + I_{REiS}\left[\exp\left(\frac{v_{B'E'}}{m_{REi}V_T}\right) - 1\right] \tag{3.3}$$

where I_{BEiS} and I_{REiS} are the saturation currents; m_{BEi} and m_{REi} are the non-ideality coefficients.

The quasi-static base current, injected across the emitter periphery is given by:

$$i_{jBEp} = I_{BEpS}\left[\exp\left(\frac{v_{B^*E'}}{m_{BEp}V_T}\right) - 1\right] + I_{REpS}\left[\exp\left(\frac{v_{B^*E'}}{m_{REp}V_T}\right) - 1\right] \tag{3.4}$$

where I_{BEpS} and I_{REpS} are the saturation currents; m_{BEp} and m_{REp} are the non-ideality factors.

In hard-saturation or inverse operation the current across the base-collector (BC) junction is modelled by:

$$i_{jBCi} = I_{BCiS}\left[\exp\left(\frac{v_{B'C'}}{m_{BCi}V_T}\right) - 1\right] \tag{3.5}$$

Similarly, the external BC junction is modelled by:

$$i_{jBCx} = I_{BCxS}\left[\exp\left(\frac{v_{B^*C'}}{m_{BCx}V_T}\right) - 1\right] \tag{3.6}$$

The weak avalanche effect and a planar breakdown is modelled by the current:

$$i_{AVL} = I_T \frac{f_{AVL}V_{DCi}}{C_c^{1/z_{Ci}}} \exp\left(-\frac{q_{AVL}}{C_{jCi0}V_{DCi}} C_c^{1/z_{Ci}-1}\right) \tag{3.7}$$

where

$$C_c = C_{jCi}(v_{B'C'})/C_{jCi0} \tag{3.8}$$

The emitter-base tunnelling current is given as:

$$i_{BEt} = I_{BEtS}(-V_e)C_e^{1-1/z_E} \exp\left[-a_{BEt}C_e^{1/z_E-1}\right] \tag{3.9}$$

where I_{BEtS} and a_{BEt} are model parameters; C_e equals $C_{jE}(v)/C_{jE0}$.

The parasitic substrate transistor current is modelled by:

$$i_{TS} = I_{TSf} - I_{TSr} = I_{TSS}\left[\exp\left(\frac{v_{B^*C'}}{m_{Sf}V_T}\right) - \exp\left(\frac{v_{S^*C'}}{m_{Sr}V_T}\right)\right] \tag{3.10}$$

where I_{TSS} is the saturation current; m_{Sf} and m_{Sr} are the emission coefficients.

In case of a forward biased SC junction, the current component is modelled by the diode equation:

$$i_{jSC} = I_{SCS}\left[\exp\left(\frac{v_{S^*C'}}{m_{SC}V_T}\right) - 1\right] \tag{3.11}$$

where I_{SCS} is the saturation current; m_{SC} is the emission coefficient.

To summarize and to give the reader some quantitative impression about the used transistors performance, some plots based on the available models are presented below. The transistor with effective emitter area of $2 \times 1.02\ \mu m \times 39.72\ \mu m$ is used.

Fig. 3.3 shows Gummel characteristics of the transistor. The transistor has the typical current gain of 90.

The maximum simulated transit frequency is 31 GHz at a collector base voltage of 1 V. It occurs for the collector current density of 0.28 $mA/\mu m^2$ (see Fig. 3.4).

The highest simulated maximum oscillation frequency is 65 GHz at the same bias point as the maximum simulated transit frequency (see Fig. 3.5).

Fig. 3.6 shows the simulated gains versus frequency at a bias where the maximum oscillation frequency has its optimum.

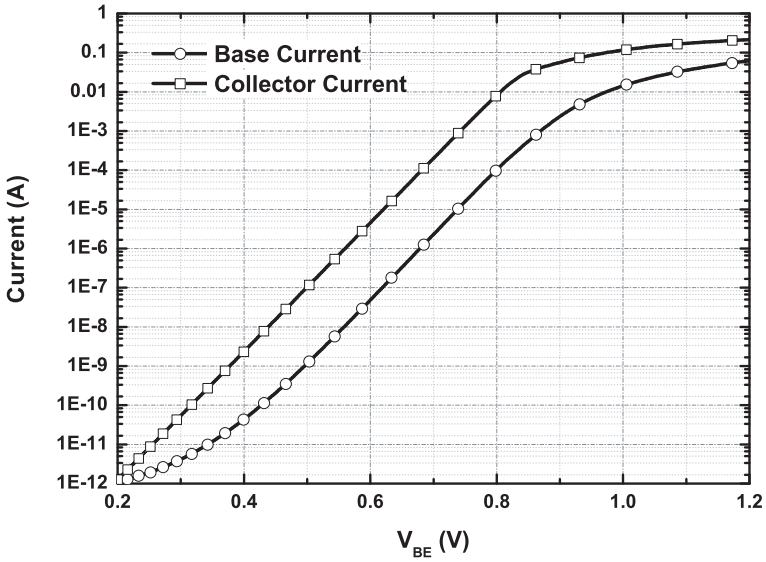


Figure 3.3: Gummel plot ($A_E = 2 \times 1.02\ \mu m \times 39.72\ \mu m$).

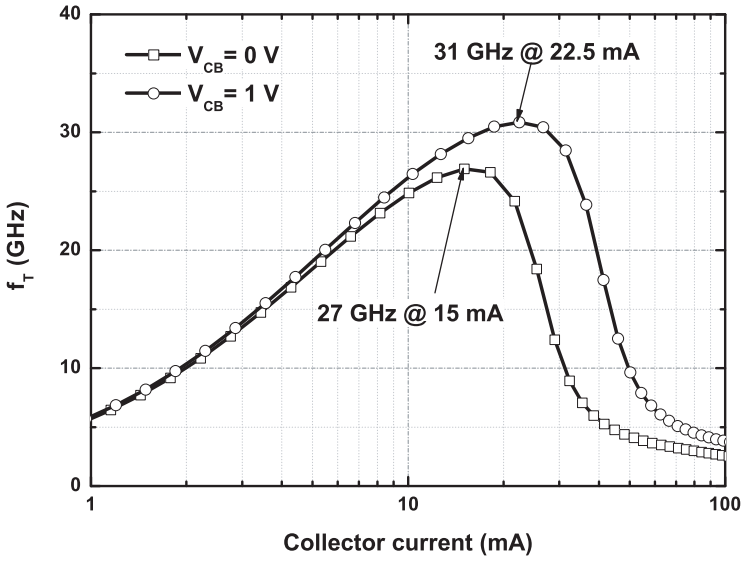


Figure 3.4: Transit frequency f_T versus collector current ($A_E = 2 \times 1.02\ \mu m \times 39.72\ \mu m$).

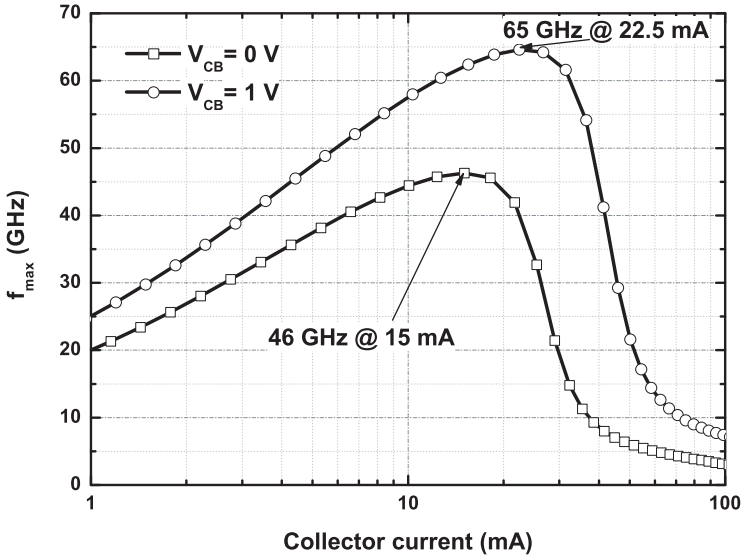


Figure 3.5: Maximum oscillation frequency f_{max} versus collector current ($A_E = 2 \times 1.02\ \mu m \times 39.72\ \mu m$).

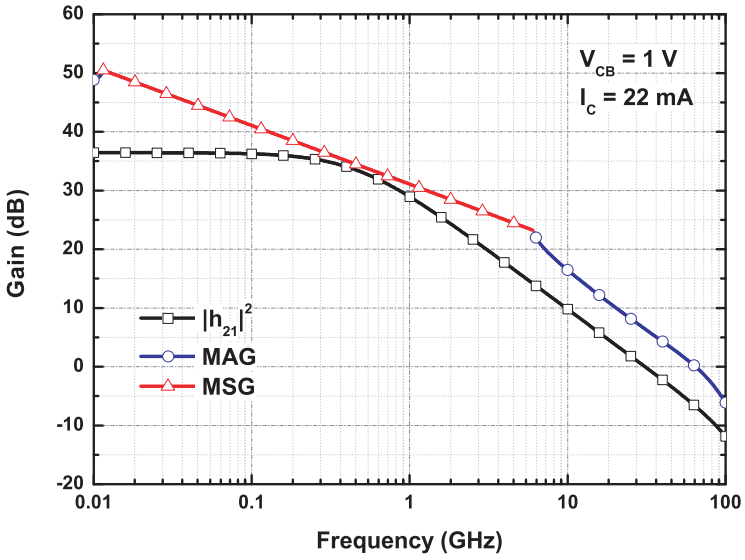


Figure 3.6: Gain versus frequency ($A_E = 2 \times 1.02\ \mu m \times 39.72\ \mu m$).

3.1.2 MOSFET Transistors

As a second option for the power amplifier design a modern 0.13 μm CMOS technology is used. This technology has four types of MOS transistors which can be divided in two groups:

- Thin gate oxide transistors with the minimum drawing gate length of 0.12 μm. Additionally this group contains three types of the devices with the different threshold voltages (low V_t, regular V_t and high V_t).
- Thick gate oxide transistors with the minimum drawing gate length of 0.4 μm.

The typical cross-section of the NMOS transistor is shown in Fig. 3.7.

Similar to the bipolar technologies the modern CMOS technologies show novel physical effects which are just included in the recently developed models. The BSIM4 is a good example of such model.

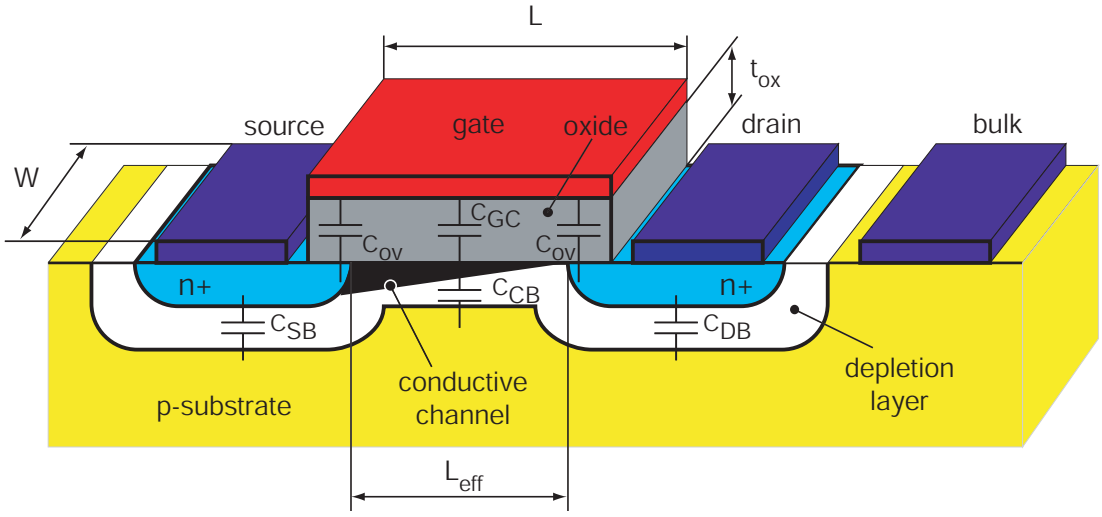


Figure 3.7: Schematic cross-section of N-channel MOSFET with parasitic capacitances.

Equivalent Circuit

The *B*erkeley *S*hort-Channel *I*GFET *M*odel, referred as BSIM, places less emphasis on the exact physical formulation of the device, but instead relies on empirical parameters and polynomial equations to handle various physical effects [Ytterdal 03].

The BSIM4 model provides different equivalent circuit configurations that are controlled by the model parameters. As active device modelling is beyond the

scope of this work, here just one option that was supplied by a design kit is considered. The large-signal BSIM4 equivalent circuit for the case when $rdsMod = 0$, $rgateMod = 0$ (no gate resistance), and $rbodyMod = 0$ (no substrate network) is show in Fig. 3.8. For the case when $rdsMod = 0$ and $R_{DS}(V) \neq 0$, the series source/drain resistance components are embedded in the I-V equation instead of the "real" physical resistance components in the model implementation. So the impact of the source/drain resistance components is modelled in dc but not in AC as well as in the noise simulation.

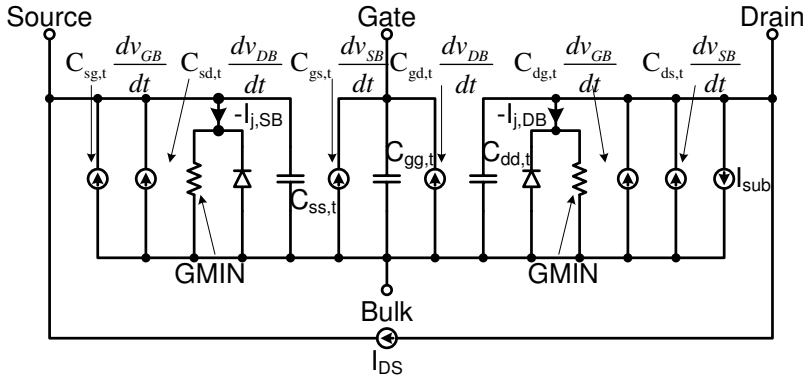


Figure 3.8: Large-signal BSIM4 equivalent circuit ($rdsMod = 0$, $rgateMod = 0$, and $rbodyMod = 0$).

The complete single equation channel current model with the contributions of velocity saturation, channel length modulation (CLM), drain induced barrier lowering (DIBL), substrate current induced body effect (SCBE) to the channel current and conductance, and drain induced threshold shift (DITS) caused by pocket implantation have been included and is given by [Liu 01]:

$$\begin{aligned} I_{ds} &= \frac{I_{ds0}}{1 + R_{DS} I_{ds0}/V_{dseff}} \left[1 + \frac{1}{C_{CLM}} \ln\left(\frac{V_A}{V_{ASAT}}\right)\right] \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ADIBL}}\right) \\ &\times \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ADITS}}\right) \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}}\right) \end{aligned} \tag{3.12}$$

where $V_A = V_{ASAT} + V_{ACLM}$.

In (3.12), I_{ds0} is the channel current for an intrinsic device (without including the source/drain resistance) in the regions from strong inversion to subthreshold which is given as:

$$I_{ds0} = \frac{W_{eff} \cdot \mu_{eff} \cdot C'_{ox,IV}}{L_{eff}\left[1 + (\mu_{eff} V_{dseff})/(2VSAT \cdot L_{eff})\right]} \cdot V_{gsteff} \cdot V_{dseff} \cdot (1 - V_{dseff}/2V_b) \tag{3.13}$$

where

$$V_b = \frac{V_{gsteff} + 2kT/q}{A_{bulk}} \tag{3.14}$$

The single equation approach that is used in the BSIM4 model for the channel current modelling is described in Appendix B in more detail.

The substrate current is given by:

$$\begin{aligned} I_{sub} &= \left(\frac{ALPHA0}{L_{eff}} + ALPHA1\right)(V_{ds} - V_{dseff}) \exp\left(-\frac{BETA0}{V_{ds} - V_{dseff}}\right) \\ &\times \frac{I_{ds0}}{1 + R_{DS} I_{ds0}/V_{dseff}} \left[1 + \frac{1}{C_{CLM}} \ln\left(\frac{V_A}{V_{ASAT}}\right)\right] \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ADIBL}}\right) \\ &\times \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ADITS}}\right) \end{aligned} \tag{3.15}$$

Table 3.1: Symbol explanation.

Symbol	Description
A_{bulk}	Factor to describe the bulk charge
$ALPHA0$	First parameter of the substrate current due to impact ionization
$ALPHA1$	Modified first parameter to account for length variation in the calculation of I_{sub}
$BETA0$	Second parameter of the substrate current due to impact ionization
C_{CLM}	Channel length modulation coefficient
$C'_{ox,IV}$	Effective oxide capacitance for I-V calculation
L_{eff}	Effective channel length
R_{DS}	Source/drain resistance
V_{ACLM}	Early voltage for the CLM effect
V_{ADIBL}	Early voltage for the DIBL effect
V_{ADITS}	Early voltage for the DITS effect
V_{ASAT}	Early voltage at the saturation voltage point
V_{ASCBE}	Early voltage for the SCBE effect
V_{ds}	Drain to source voltage
$VSAT$	Saturation velocity
V_{dseff}	Effective drain to source voltage
V_{gsteff}	Effective $V_{GS} - V_T$ smoothing function
W_{eff}	Effective channel width
μ_{eff}	Effective mobility

Total device capacitances referred to Fig. 3.8 are given as following [Liu 01]:

$$C_{gg,t} = C_{gg} + C_{ov,GS} + C_{f,GS} + C_{ov,GD} + C_{f,GD} + C_{gb,0} \tag{3.16}$$

$$C_{gd,t} = C_{gd} + C_{ov,GD} + C_{f,GD} \tag{3.17}$$

$$C_{gs,t} = C_{gs} + C_{ov,GS} + C_{f,GS} \tag{3.18}$$

$$C_{gb,t} = C_{gb} + C_{gd,0} \tag{3.19}$$

$$C_{dg,t} = C_{dg} + C_{ov,GD} + C_{f,GD} \tag{3.20}$$

$$C_{dd,t} = C_{dd} + C_{ov,GD} + C_{f,GD} + C_{j,DB} \tag{3.21}$$

$$C_{ds,t} = C_{ds} \tag{3.22}$$

$$C_{db,t} = C_{db} + C_{j,DB} \tag{3.23}$$

$$C_{sg,t} = C_{sg} + C_{ov,GS} + C_{f,GS} \tag{3.24}$$

$$C_{sd,t} = C_{sd} \tag{3.25}$$

$$C_{ss,t} = C_{ss} + C_{ov,GS} + C_{f,GS} + C_{j,SB} \tag{3.26}$$

$$C_{sb,t} = C_{sb} + C_{j,SB} \tag{3.27}$$

$$C_{bg,t} = C_{bg} + C_{gb,0} \tag{3.28}$$

$$C_{bd,t} = C_{bd} + C_{j,DB} \tag{3.29}$$

$$C_{bs,t} = C_{bs} + C_{j,SB} \tag{3.30}$$

$$C_{bb,t} = C_{bb} + C_{j,DB} + C_{j,SB} + C_{gb,0} \tag{3.31}$$

The subscripts SB and DB for fringing capacitance are for readability purpose because the BSIM4 does not distinguish between the fringing capacitance at the source side and drain side.

The set of the standard simulations are made to show the performance of the used technology. For this purpose the transistor configuration with the drawing width of 100 μm, length of 0.12 μm and 20 fingers is used for the thin oxide devices. The thick oxide device has the same width to length ratio as the thin one (width of 330 μm, length of 0.4 μm and 20 fingers).

The transfer characteristics for all types of the NMOS transistors are shown in Fig. 3.9.

Fig. 3.10 shows that the thin gate oxide devices have the maximum oscillation frequency above 120 GHz and the thick gate oxide transistor has the maximum oscillation frequency above 30 GHz.

The gain frequency responses at the bias points where the highest maximum oscillation frequency occurs are shown in Fig. 3.11.

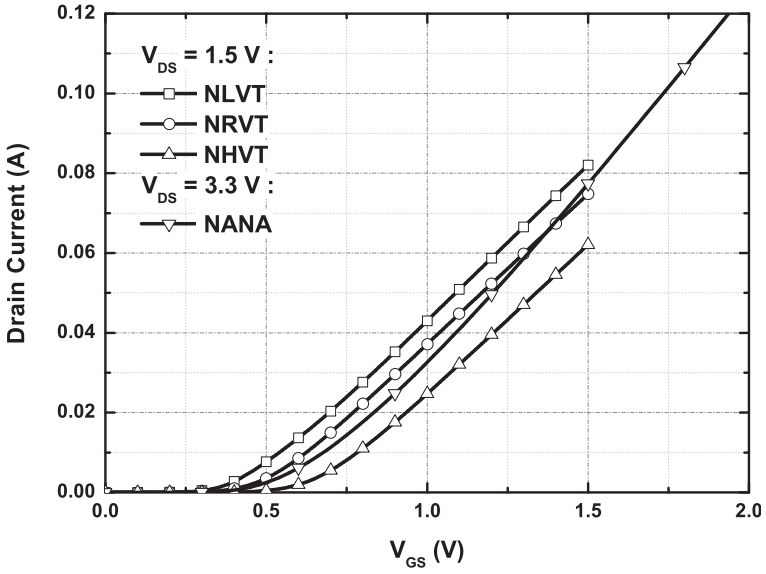


Figure 3.9: Transfer characteristic ($A_{G\_NLVT} = A_{G\_NREG} = A_{G\_NHVT} = 100\ \mu m \times 0.12\ \mu m$; $A_{G\_NANA} = 330\ \mu m \times 0.4\ \mu m$).

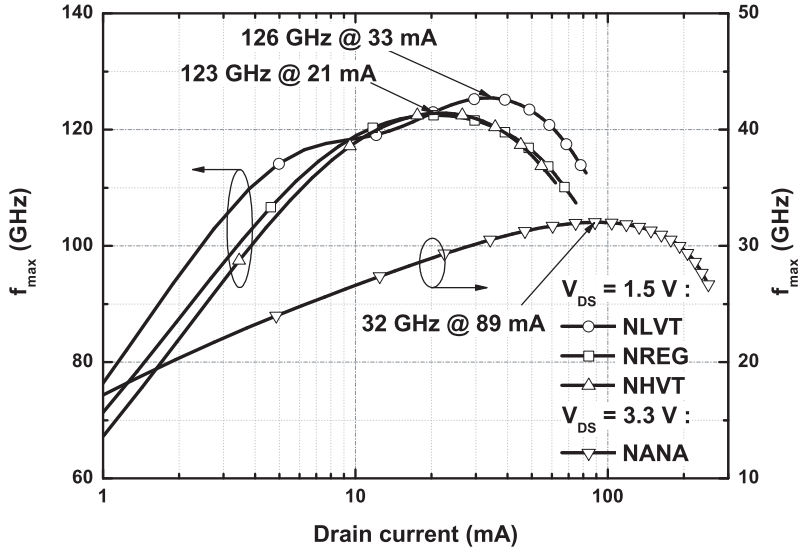


Figure 3.10: Maximum oscillation frequency f_{max} versus drain current ($A_{G\_NLVT} = A_{G\_NREG} = A_{G\_NHVT} = 100\ \mu m \times 0.12\ \mu m$; $A_{G\_NANA} = 330\ \mu m \times 0.4\ \mu m$).

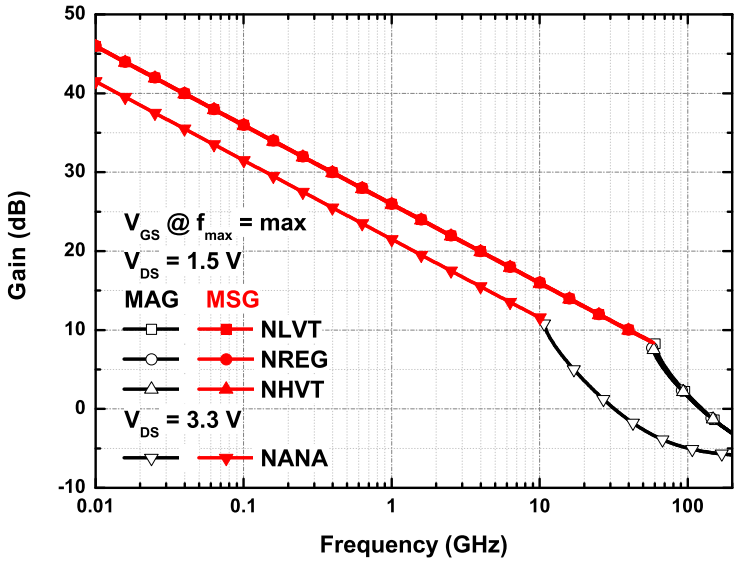


Figure 3.11: Gain versus frequency ($A_{G\_NLVT} = A_{G\_NREG} = A_{G\_NHVT} = 100\ \mu m \times 0.12\ \mu m$; $A_{G\_NANA} = 330\ \mu m \times 0.4\ \mu m$).

3.2 Passive Components

A typical cross section of the standard CMOS process is presented in Fig. 3.12. It consists of several metal layers above the silicon substrate. Normally the higher the layer, the greater is the thickness. The top layer in this technology is a thick aluminium layer and all others are copper layers. In between, the space is filled by silicon oxide and above it is covered by polyimide, except of the pad openings.

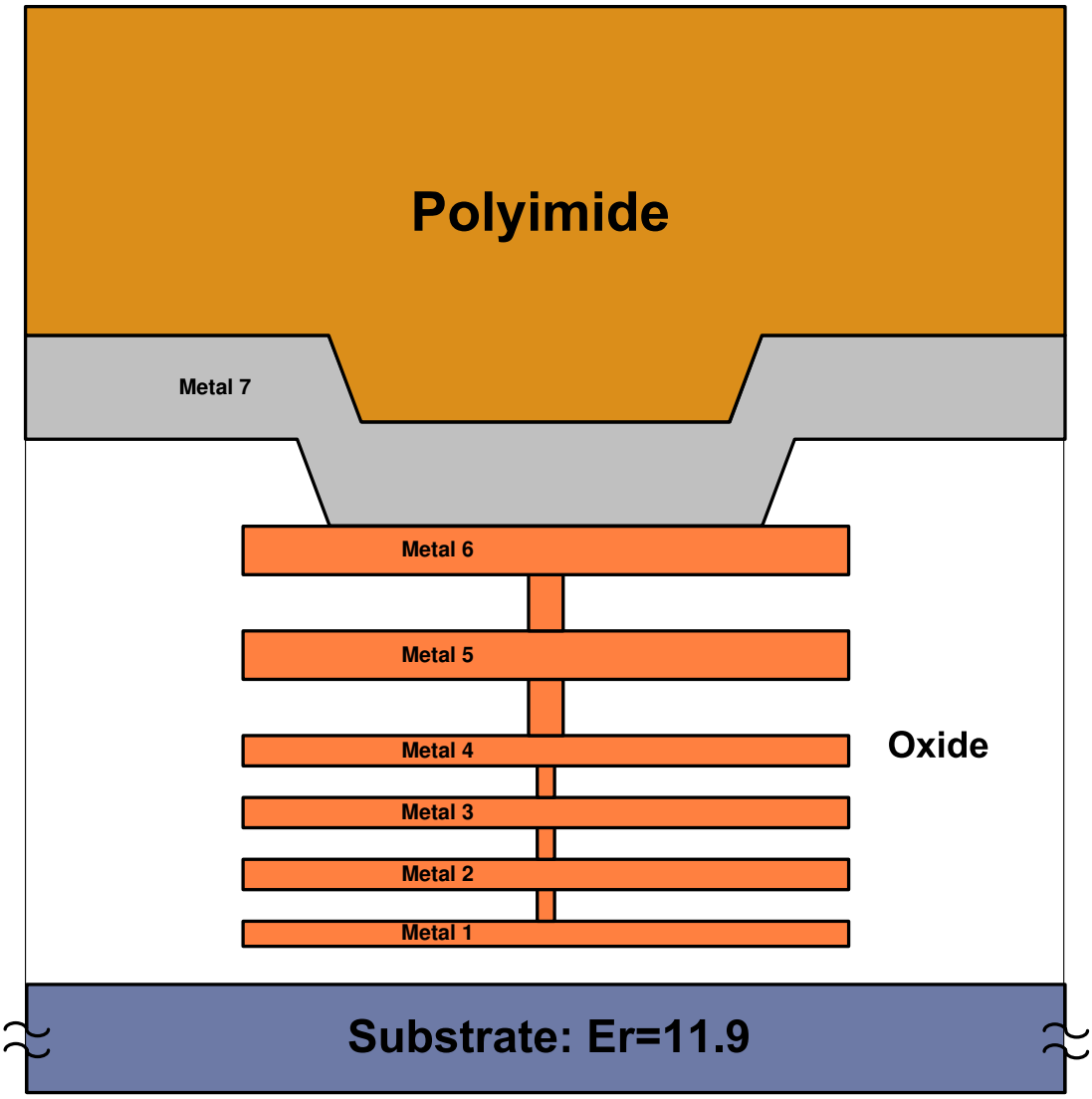


Figure 3.12: Proportional schematic cross-section of a standard digital CMOS process, showing an available metal stack that can be used for the design of passive elements.

3.2.1 Capacitors

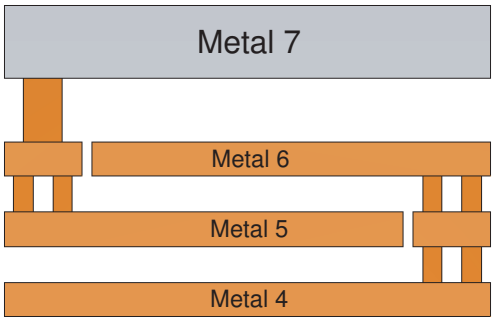
Capacitors are essential components in the present work. They are used as a short for bypassing and coupling RF signal and as a reactance in matching networks. There are four types of capacitor which are commonly used in MMIC design: gate capacitors, junction capacitors, metal-to-metal/poly capacitors, and thin-insulator capacitors. The gate and junction capacitors are nonlinear, have a lower breakdown voltage, lower quality factor (Q) and higher capacitance density in comparison with other capacitor types. Additionally they require dc biasing. The metal-to-metal/poly and thin-insulator capacitors are linear, have a higher Q, but suffer from the lower capacitance density in comparison with the gate and junction capacitors.

Table 3.2: Comparison table of capacitors [Aparicio 02].

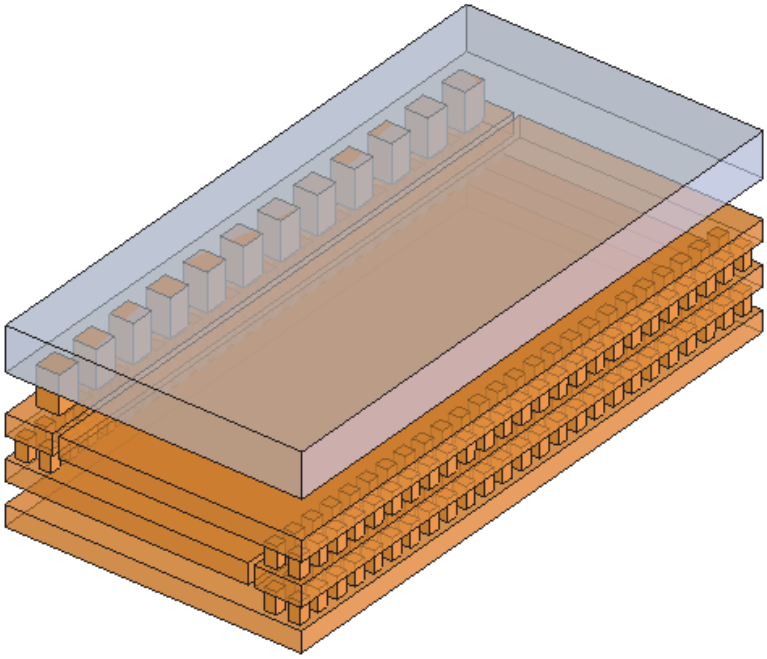
Structure	**Capacitance Density** ($aF/\mu m^2$)	**Average** (pF)	**Area** (μm^2)	**Capacitance Enhancement**	f_{res} (GHz)	**Q** @ 1 GHz	**Break Down** (V)
VPP	1512.2	1.01	669.9	7.4	>40	83.2	128
HPP	203.6	1.09	5378.2	1	21	63.8	500
MIM	1100	1.05	960.9	5.4	11	95	

Table 3.2 gives an overview of some popular metal-to-metal and thin-insulator capacitor configurations. The results of this table are based on the structure produced in a purely digital 7 metal layer CMOS technology [Aparicio 02]. The Horizontal Parallel Plate (HPP) structure has a lowest capacitance density. The improved version of the HPP structure is a Metal-Insulator-Metal (MIM) or thin-insulator structure, this structure has much higher capacitance density and requires the additional production step to produce it and suffer from a lower breakdown voltage. Vertical Parallel Plate(VPP) structure is a good alternative to MIM and HPP structures, but it is not always available in the design flow.

Fig. 3.13 shows HPP capacitor which consists of three capacitors connected in parallel formed by four metal layers. The linear lumped model for the capacitor is shown in Fig. 3.14. It is tree pin model which consists of a main capacitor (C) in series with a parasitic inductance (L_s) and resistance (R_s); and other parasitic components to ground (C_{p1}, C_{p2}, R_{sub1}, R_{sub2}, C_{sub1}, C_{sub2}). Depending on the implementation, the lumped capacitor model can be further simplified.



(a)



(b)

Figure 3.13: Horizontal parallel plate capacitor: (a) Front View; (b) 3D View.

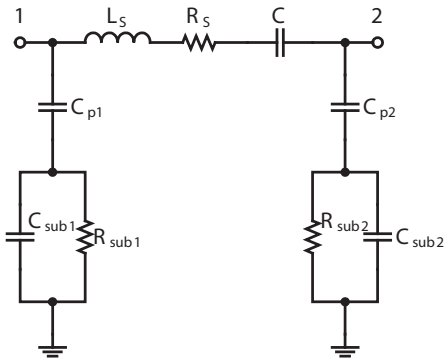
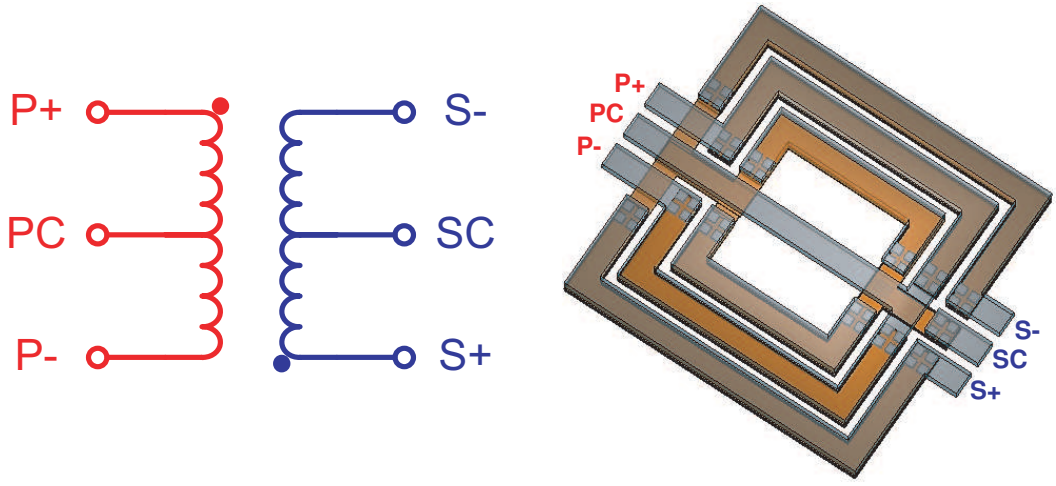


Figure 3.14: RF capacitor lumped model.

3.2.2 Transformers

Monolithically integrated transformers are the key components in this work; they are used as a matching network, balanced to unbalanced convertors and vise versa, dc decouplers, resonators, tuned networks for feedback. All power amplifiers, realised in this work, use transformers for the input, output and interstage matching as well as power combining and dividing networks with tuned properties.



(a) (b)

Figure 3.15: Symmetrical square-shaped transformer: (a) Schematic symbol; (b) 3D View.

Fig. 3.15 shows a symmetrical square-shaped transformer with a centre-tapped connection on both windings.

There are two popular models of the transformer: first is a lumped model derived from the physical layout and process technology, second is a scattering (S) parameters model obtained from measurement or Electro-Magnetic (EM) simulation.

An example of the lumped transformer model [Simbuerger 99,a] is shown in Fig. 3.16. The elements of this model can be identified as:

- Multiple coupled inductors of the windings ($L1$, $L2$, $L3$, $L4$) and coupling coefficients between them ($k12$, $k13$, $k14$, $k23$, $k24$, $k34$).
- Ohmic loss in the conductor material due to skin effect, current crowding and finite conductivity ($R3$, $R4$, $R7$, $R8$).
- Parasitic capacitive coupling between the windings ($C4$, $C5$, $C6$, $C7$).
- Parasitic capacitive coupling into the substrate ($C1$, $C2$, $C3$, $C8$, $C9$, $C10$).
- Losses in the conductive substrate ($R1$, $R2$, $R5$, $R6$, $R9$, $R10$).

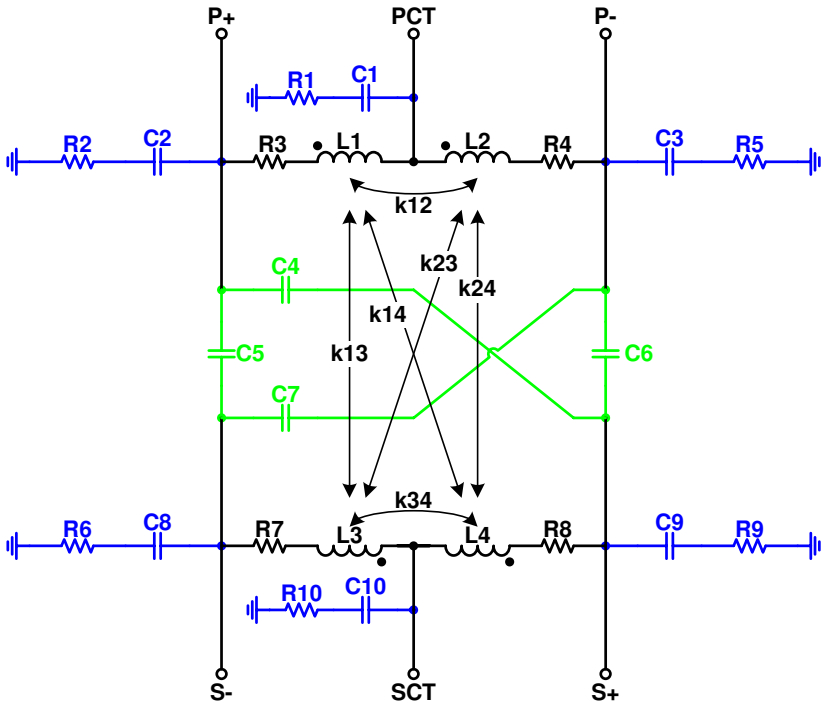


Figure 3.16: RF transformer lumped model.

The lumped component model described above has two main drawbacks:

- It is not broad band enough for applications (e.g. power amplifier) where second, third harmonics etc. play an important role on a circuit performance.
- It is symmetrical and could require component values adjustment for asymmetrical use.

To improve the above, more complicated lumped model or S parameters model can be used instead.

The S parameters model can be represented as a simplified lumped transformer model (Fig. 3.17(a)) or by the T-network (Fig. 3.17(b)).

The values of the primary and secondary self inductance are given by:

$$L_p = \frac{\Im(Z_{11})}{\omega} \tag{3.32}$$

and

$$L_s = \frac{\Im(Z_{22})}{\omega} \tag{3.33}$$

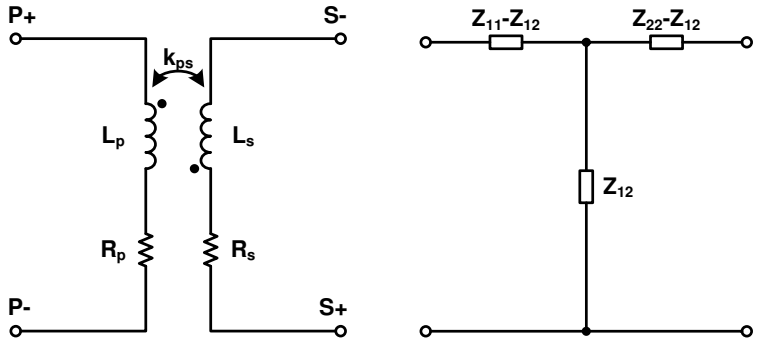


Figure 3.17: S parameters representation: (a) Lumped transformer; (b) T-network (Z_{12}=Z_{21}).

The primary and secondary series resistance are given as:

$$R_p = \Re(Z_{11}) \tag{3.34}$$

and

$$R_s = \Re(Z_{22}) \tag{3.35}$$

The mutual inductance between primary and secondary windings is given by:

$$M_{ps} = \frac{\Im(Z_{12})}{\omega} \tag{3.36}$$

Whereas the coupling coefficient can be expressed as:

$$k_{ps} = \frac{M_{ps}}{\sqrt{L_p L_s}} = \frac{\Im(Z_{12})}{\sqrt{\Im(Z_{11})\Im(Z_{22})}} \tag{3.37}$$

This lumped model representation is valid at the frequency range where a core resistive loss due to the substrate conductivity can be neglected ($\Re(Z_{12}) = 0$), but it still can be used as a handling tool for other frequency ranges.

Another parameter that can help to compare or characterise transformers is the quality factor.

The quality factor of the primary and secondary windings when the counter winding is open can be calculated using the following expressions:

$$Q_{op} = \frac{\Im(Z_{11})}{\Re(Z_{11})} \tag{3.38}$$

and

$$Q_{os} = \frac{\Im(Z_{22})}{\Re(Z_{22})} \tag{3.39}$$

The second definition of the quality factors are when the counter winding is shorted and are given by:

$$Q_{sp} = \frac{\Im(\frac{1}{Y_{11}})}{\Re(\frac{1}{Y_{11}})} \tag{3.40}$$

and

$$Q_{ss} = \frac{\Im(\frac{1}{Y_{22}})}{\Re(\frac{1}{Y_{22}})} \tag{3.41}$$

The real quality factor is when the transformer is embedded in to the circuit and the value is lying in-between.

3.2.3 Bond Wires

Monolithic millimetre-wave integrated circuits requires some interface to connect the inputs and outputs to the external world. One of the alternatives to create such interface is the usage of bond wires. The bond wires can be of different materials (gold or aluminium) with different diameters (12 μm, 25 μm etc.) and can have different forms (3D routing). Fig. 3.18(a) shows an example of two coupled bond wires which connect output of the power amplifier (MMIC) to the 50 Ω microstrip line.

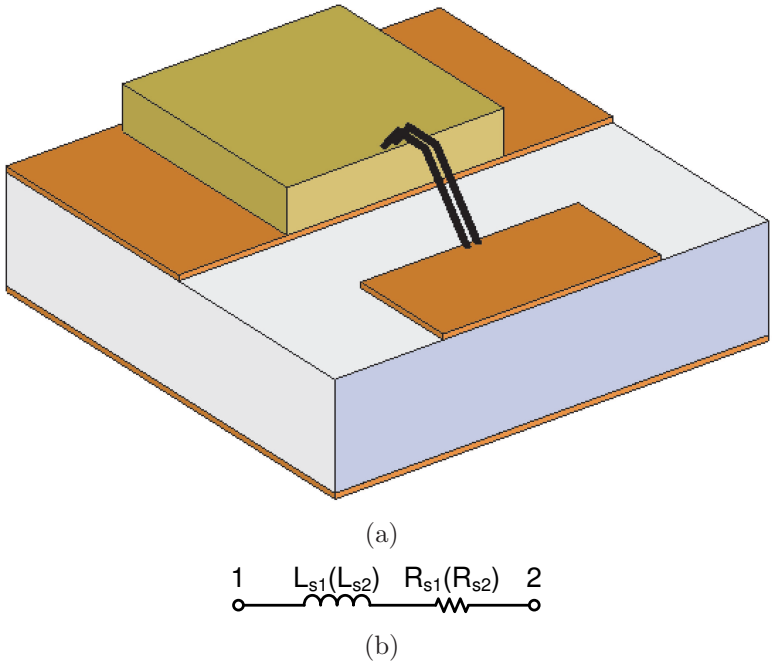


Figure 3.18: Bond wires: (a) 3D view; (b) RF lumped model.

The RF lumped model, used for modelling bond wires, is shown in Fig. 3.18(b). The model consists of an inductor connected in series with the resistor. The parasitic capacitance of the bond wire in most cases can be neglected. The model values can be extracted from the measurement, 3D EM simulation or can be calculated analytically.

Chapter 4

Power Amplifier Design Guide

The design of the power amplifier is always a trade-off between the output power, efficiency, gain, linearity etc. There is no one solution when all these parameters reaches the best performance simultaneously so a trade-off analysis has to be performed. The trade-off analysis leads to choice of the class of the operation, technology of the implementation, active device size, operating point and matching network configuration. The theory about the power amplifier classes (see 2) gives an overview about the properties of the power amplifier classes based on the ideal device assumption. Hence the analysis when the real devices are used is required.

This part describes the design procedure (see Fig. 4.1) of the CMOS (based on BSIM4.2 model) and Bipolar (based on HICUM v2.1 model) transformer-based Class-A, Class-AB and Class-B power amplifiers when the power added efficiency is used as a figure of merit.

The power amplifier design procedure is split into four steps:

- Design of the power amplifier prototype.
- Load-pull analysis of the prototype amplifier.
- Design of the transformer-based matching network.
- Design of the final transformer-based linear push-pull power amplifier.

All these steps are described below in more detail.

The Advanced Design System 2005A is used to perform routine calculations.

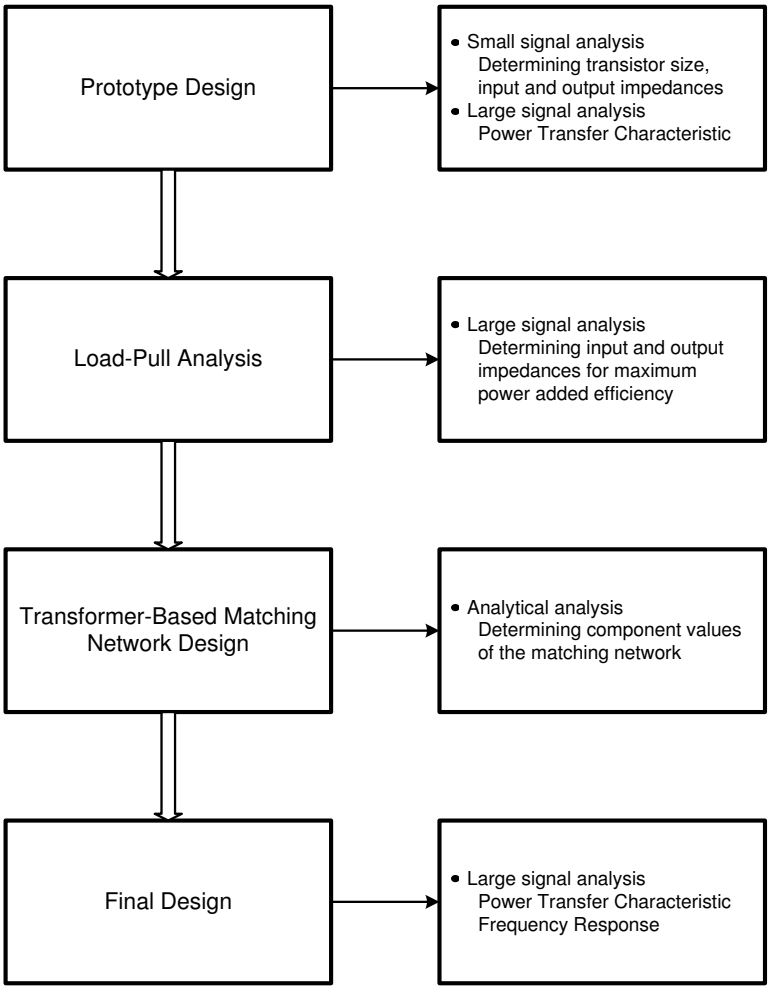


Figure 4.1: Power amplifier design procedure.

4.1 Prototype Design

4.1.1 CMOS Power Amplifier

Fig. 4.2 shows the test bench used for the CMOS power amplifier design. It consists of the NMOS transistor $M1$, two swept dc sources VG and $Supply$, controls required to perform simulation and set of variables which control the simulation.

The variables are:

- $Width$ is the total width of the transistor in μm.
- $Finger\_Width$ is the width of the one finger in μm.
- $Length$ is the length of the transistor in μm.
- $PoutdBm\_spec$ is the required output power in dBm.
- $RFreq$ is the operating frequency in Hz.
- $Temperature$ is the operating temperature in °C.
- VDD_start, VDD_stop, VDD_step are the start, stop and step values for the drain voltage sweep in V.
- Vg_start, Vg_stop, Vg_step are the start, stop and step values for the gate voltage sweep in V.

The simplified BSIM4 large-signal equivalent circuit in common source configuration with source and bulk connected together is shown in Fig. 4.3. As the source and bulk are connected all elements between source and bulk plus elements which contain a dv_{SB}/dt multiplier are omitted, the gate resistor (R_g) is added to fulfil high frequency response.

The gate resistance is defined by the transistor geometry and is given by:

$$R_g = \frac{1}{3}\frac{W}{L}R_{SH,G}\frac{1}{N^2} \tag{4.1}$$

where W is the width of the transistor; L is the length of the transistor; N is the number of finger, $R_{SH,G}$ is the sheet resistance of the gate material (poly silicon); if all fingers are connected at both sides by a metal instead of at one side, then the factor 1/3 should be replaced by 1/12.

The I-V output characteristic of the Device Under Test (DUT) is shown in Fig. 4.4. Marker $m1$ determines the supply voltage V_{DD} and the output quiescent current I_{Out_Q}. Marker $m2$ determines the maximum output current I_{Out_max} and

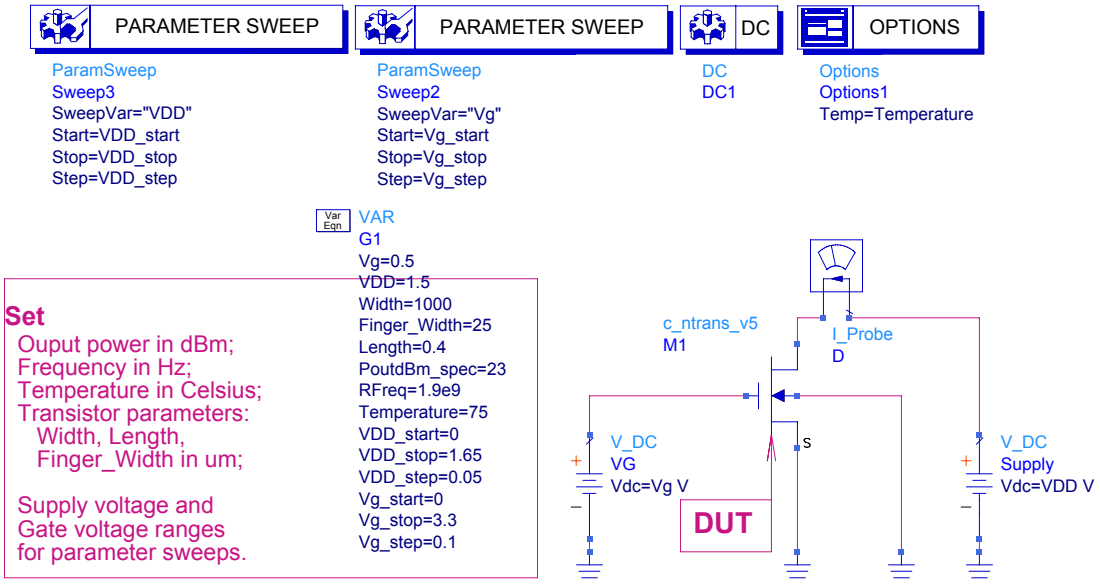


Figure 4.2: Test bench to design the CMOS power amplifier.

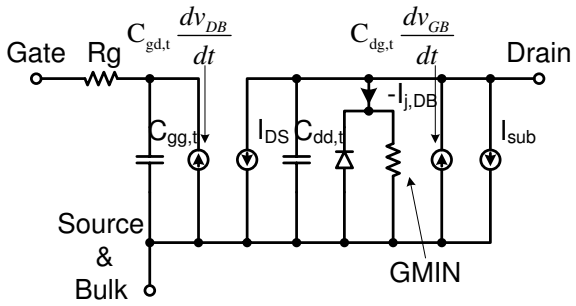


Figure 4.3: Simplified BSIM4 large-signal equivalent circuit in common source configuration with source and bulk connected together.

the amplitude of the output voltage $V_{Out} = V_{m1} - V_{m2}$, in accordance with the linear power amplifier theory given in 2.2.1.

From (2.31), the current I_{Out_Q} is defines as:

$$I_{Out\_Q} = -\frac{I_{Out\_max}\cos(\alpha/2)}{1-\cos(\alpha/2)} \tag{4.2}$$

Solving (4.2) for α gives:

$$\alpha = 2\arccos\left(\frac{I_{Out\_Q}}{I_{Out\_Q} - I_{Out\_max}}\right) \tag{4.3}$$

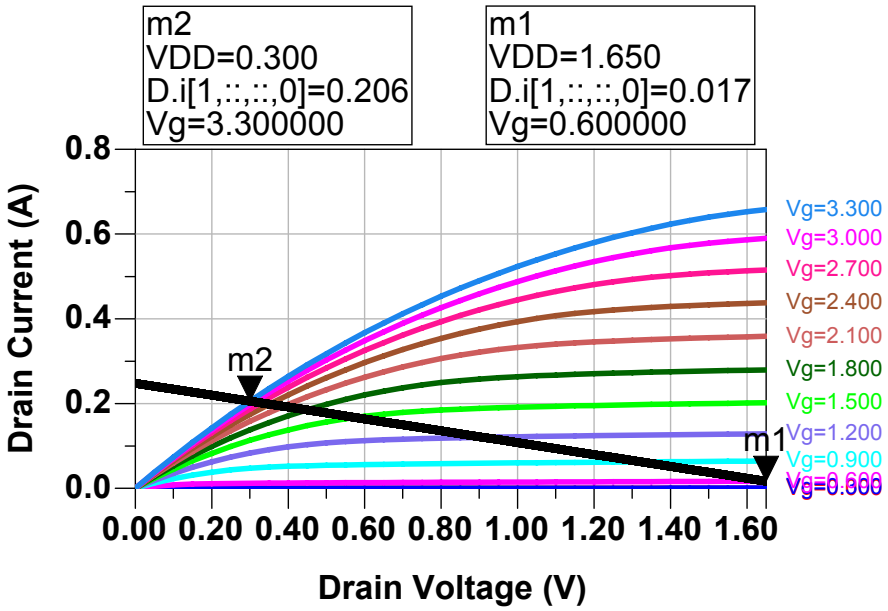


Figure 4.4: CMOS output characteristics showing the choice of the operating point and load line.

The dc current (2.35) and the current amplitude of the first harmonic (2.36) equal:

$$I_{dc}(\alpha) = \begin{cases} \frac{I_{Out\_max}}{2\pi} \frac{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}{1-\cos(\alpha/2)} & I_{Out\_max} - 2I_Q \geq 0 \\ I_Q & I_{Out\_max} - 2I_Q < 0 \end{cases} \tag{4.4}$$

and

$$I_{Out} = I_1(\alpha) = \begin{cases} \frac{I_{Out\_max}}{2\pi} \frac{\alpha - \sin(\alpha)}{1-\cos(\alpha/2)} & I_{Out\_max} - 2I_{Out\_Q} \geq 0 \\ I_{Out\_max} - I_{Out\_Q} & I_{Out\_max} - 2I_{Out\_Q} < 0 \end{cases} \tag{4.5}$$

The load resistance R_l is defined by the load line between the markers m1 and m2 (see Fig. 4.4) and output resistance r_o and is expressed as:

$$R_l = \begin{cases} \frac{V_{Out}}{I_{Out} - V_{Out}/r_o} & \left(\frac{V_{Out}}{I_{Out}} < r_o\right) \,\&\&\, (I_{Out\_max} - I_{Out\_Q} \geq 0) \\ do\ not\ consider & else \end{cases} \tag{4.6}$$

The small-signal equivalent circuit of the CMOS power amplifier is shown in Fig. 4.5. The multiplier dv_{SB}/dt was changed by $v_{in}v_{out}$. In accordance with (3.21) the drain-bulk junction capacitance ($C_{j,DB}$) has to be included into the total capacitance ($C_{dd,t}$) but the model implementation in the circuit simulators does not so the drain-bulk junction capacitance is represented by a separate capacitor ($C_{j,DB}$) (see Fig. 4.5).

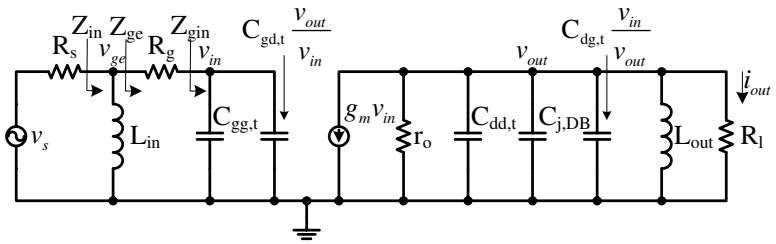


Figure 4.5: Small-signal equivalent circuit of the CMOS power amplifier.

The voltage controlled current source has to be loaded by the real impedance to get the highest efficiency. It follows that v_{in} and v_{out} has to be 180° out-of phase. Using the statement above, the total output capacitance can be calculated as:

$$\begin{aligned} C_{out} &= C_{dd,t} + C_{j,DB} + C_{dg,t}\frac{|v_{in}|}{|v_{out}|} \\ &= C_{dd,t} + C_{j,DB} + C_{dg,t}\frac{|v_{in}|}{g_m|v_{in}|(R_l||r_o)} \\ &= C_{dd,t} + C_{j,DB} + C_{dg,t}\frac{(R_l + r_o)}{g_m R_l r_o} \end{aligned} \tag{4.7}$$

where $C_{dd,t}$, $C_{j,DB}$, $C_{dg,t}$ and g_m are defined by the operating point.

The output inductance (L_{out}) equals:

$$L_{out} = \frac{1}{\omega_o^2 C_{out}} \tag{4.8}$$

where ω_o is an operating frequency.

Using properties of v_{in} and v_{out} the total input capacitance and input impedance can be expressed as:

$$C_{in} = C_{gg,t} + C_{gd,t}\frac{|v_{out}|}{|v_{in}|} = C_{gg,t} + \frac{C_{gd,t} g_m R_l r_o}{R_l + r_o} \tag{4.9}$$

$$Z_{in} = R_g - j\frac{1}{\omega_o C_{in}} \tag{4.10}$$

The conjugate matching theory is used to find the value of the components R_s and L_{in} as:

$$L_{in} = \frac{1}{\Im\left(1/Z_{in}\right)\omega_o} \tag{4.11}$$

and

$$R_s = \frac{1}{\Re\left(1/Z_{in}\right)} \tag{4.12}$$

Finally, to design a prototype the supply voltage, the operating point and a load line have to be chosen. The supply voltage is chosen as a half of the maximum specified drain source voltage for the transistor. The operating point and load line are chosen after analysis of the estimated output power (Fig. 4.6), drain efficiency (Fig. 4.7) and power added efficiency (Fig. 4.8).

By the definition the output power equals:

$$P_{Out} = \frac{V_{Out}^2}{2R_l} \tag{4.13}$$

where V_{Out} is an amplitude of the output voltage $(V_{m1} - V_{m2})$ and R_l is expressed in (4.6).

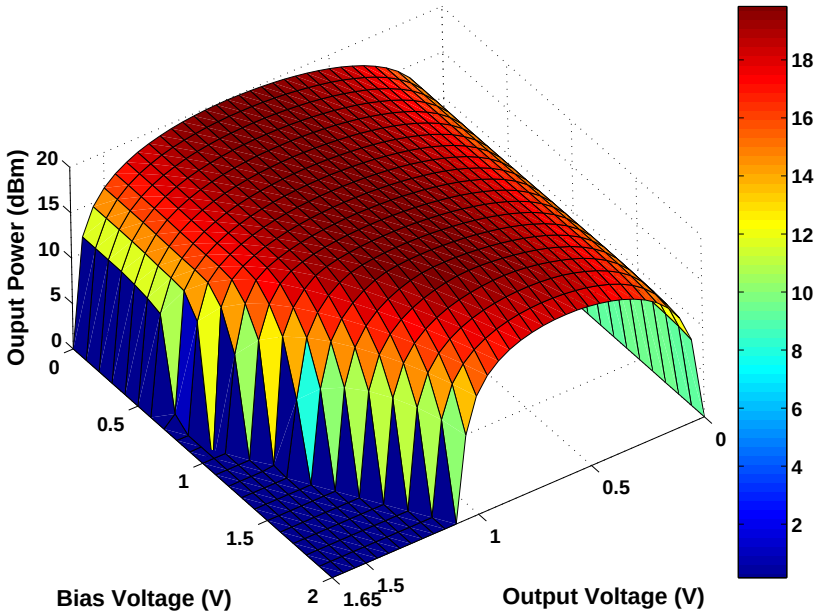


Figure 4.6: Expected output power based on the analysis of the CMOS output characteristics as a function of the chosen operating point and load line.

Fig. 4.6 shows the output power above 0 dBm to make the graph more readable.

The drain efficiency is defined as:

$$\eta = \frac{P_{Out}}{V_{dc} I_{dc}} \tag{4.14}$$

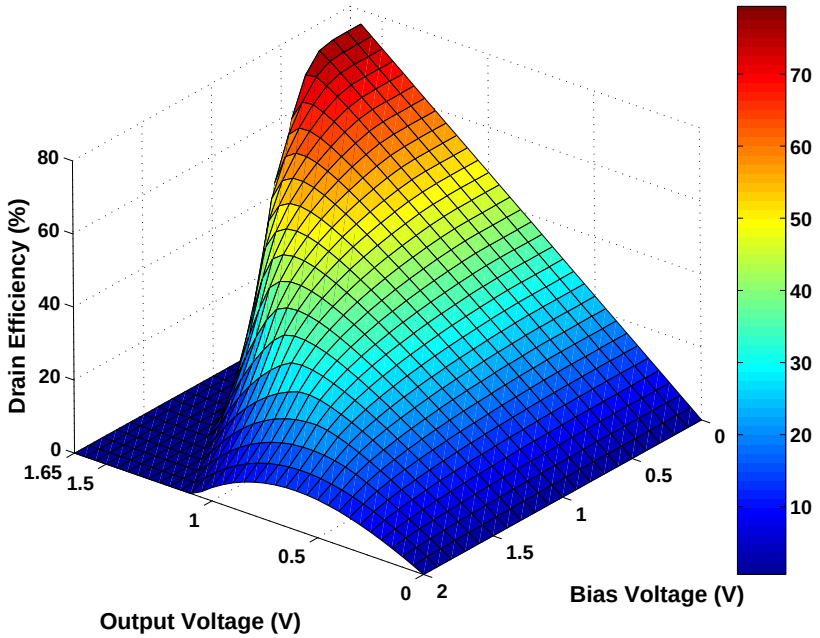


Figure 4.7: Estimated drain efficiency based on the analysis of the CMOS output characteristics as a function of the chosen operating point and load line.

Fig. 4.7 shows that the drain efficiency reaches its theoretical maximum $\frac{\pi}{4}$ (Class-B) when the bias voltage is 0 V and the amplitude of the output voltage equals to the supply voltage but such condition leads to the vanish of the output power.

An estimation of the power added efficiency requires an information about the input power or transducer power gain. Usually, the power amplifier has the highest efficiency at the saturation so the saturated transducer power gain is required. The saturated power gain requires a large-signal analysis that makes the analytical calculations more complex. Thus the small-signal transducer power gain with compression coefficient g_c is introduced instead:

$$g_t = g_c \frac{p_{out}}{p_{in}} = g_c \frac{R_s \left[g_m (R_l || r_o)\right]^2}{R_l \left[\left(R_g \omega_o C_{in}\right)^2 + 1\right]} \tag{4.15}$$

Then the power added efficiency equals:

$$pae = \eta \left(1 - \frac{1}{g_t}\right) \tag{4.16}$$

The power added efficiency for the case when $g_c = 1$ is plotted in Fig. 4.8, showing sharp decrease when the bias voltage reaches the subthreshold region but it is not the case for the large-signal gain so the coefficient g_c has to be more then 1 for other regions large-signal gain usually less then small-signal gain and $g_c \leq 1$.

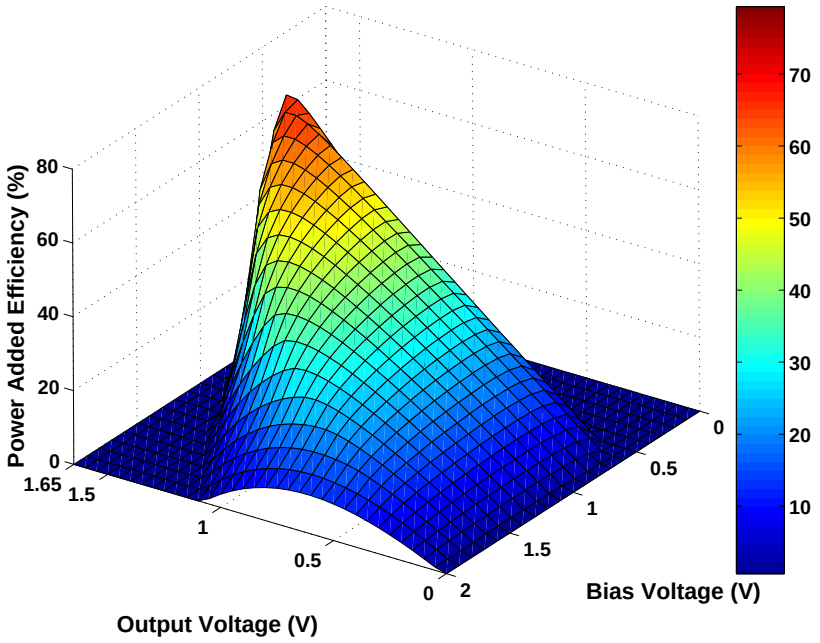


Figure 4.8: Expected power added efficiency based on the analysis of the CMOS output characteristics as a function of the chosen operating point and load line.

Let's choose the point where the power added efficiency equals to 65.7 % at the bias voltage of 0.4 V and the output voltage of 1.6 V which corresponds to the output power of 11.6 dBm and drain efficiency of 70.7 %. In case if the output power does not fulfil specification requirements the gate $Width$ has to be changed in accordance with:

$$Width = Width\frac{P_{Out\_spec}}{P_{Out}} \tag{4.17}$$

The next step is to check the designed prototype under the large-signal operation. For that the gotten component values of the source resistance $R_s = 234\ \Omega$, load resistance $R_l = 89\ \Omega$, input inductance L_{in}=3 nH, output inductance L_{out}=9.4 nH and transistor width $Width$=1000 μm as well as operating point parameters have to be set in the set block of the CMOS power amplifier test bench (see Fig. 4.9).

Fig. 4.10 shows HB simulation results of the prototype constructed before. The prototype shows performance similar to the predicted one, namely the saturated output power of 11.6 dBm with the drain efficiency of 71.8 % and power added efficiency of 66.8 %.

The drain voltage and channel current (current form the current source in the model) waveforms are shown in Fig. 4.11. The channel current is used instead of the drain current as it does not contain the current of the parasitic capacitors. The drain voltage is a pure sinus as all higher harmonics are shorted by the load

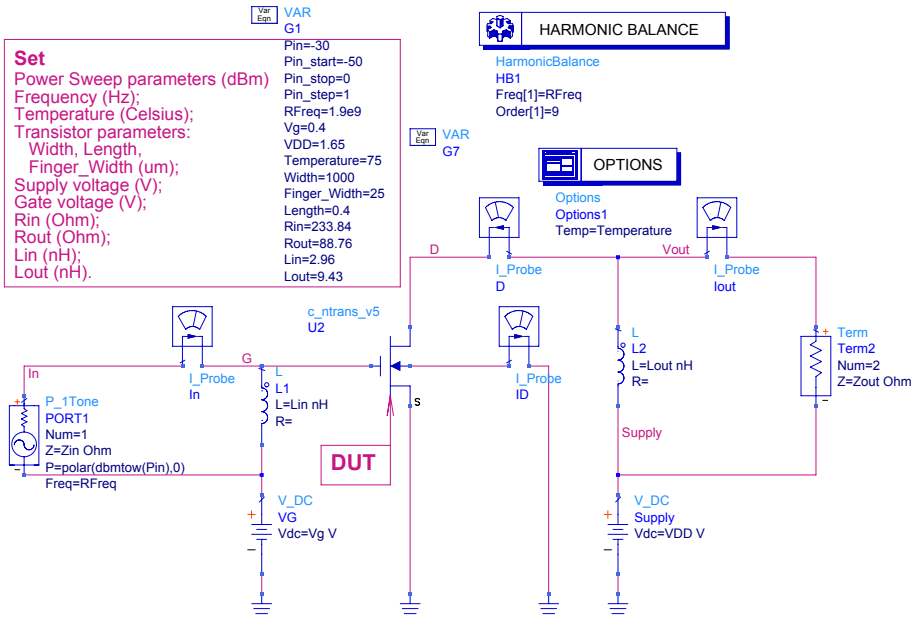


Figure 4.9: Harmonic balance test bench to design the CMOS power amplifier.

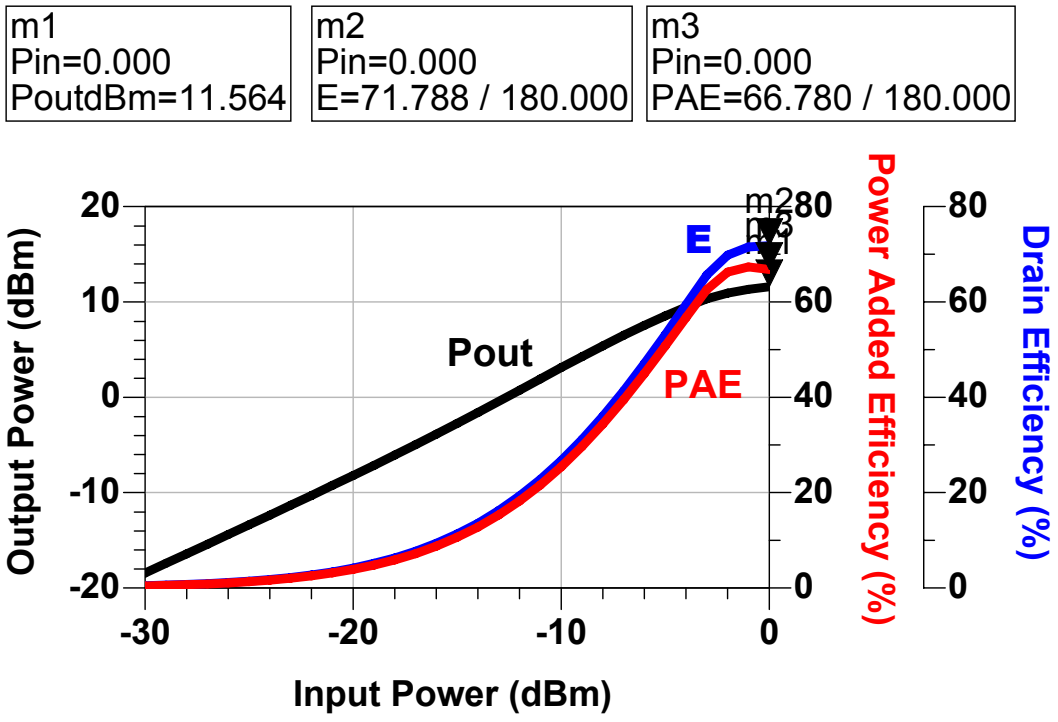


Figure 4.10: Large-signal analysis of the CMOS power amplifier prototype, showing the output power and efficiencies as a function of the input power.

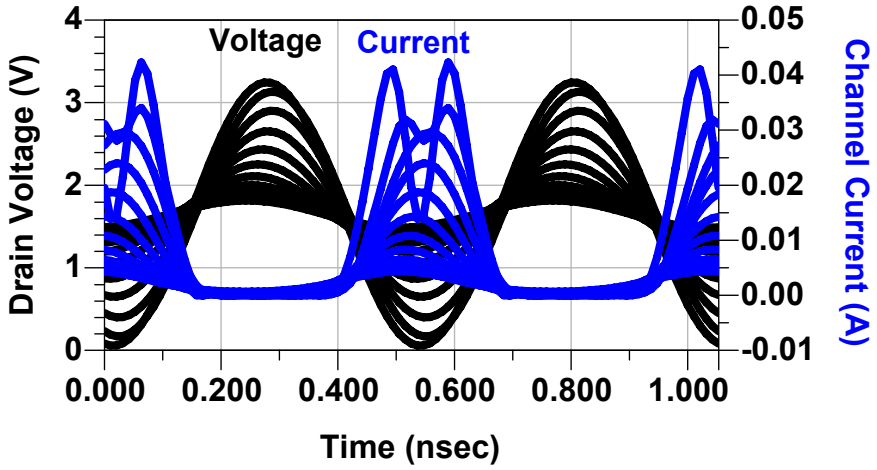


Figure 4.11: Time domain representation of the drain voltage and channel current of the designed CMOS power amplifier prototype.

and the knee voltage and high drain voltage swing cause of a bifurcated form of the channel current. The dynamic load lines for the different input powers can be plotted as the channel current waveform versus drain voltage waveform (see Fig. 4.12).

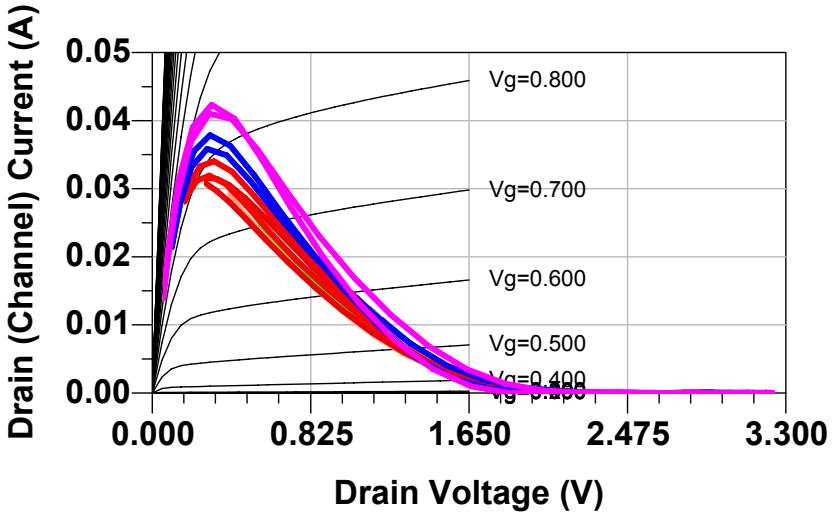


Figure 4.12: Dynamic load lines of the designed CMOS prototype power amplifier, showing that the amplifier operates similar to the ideal Class-B amplifier.

4.1.2 Bipolar Power Amplifier

Fig. 4.13 shows a test bench used for the Bipolar power amplifier design. It consists of the NPN transistor $T1$, two swept dc sources VB and $Supply$, controls required to perform the simulation and set of variables which control the simulation.

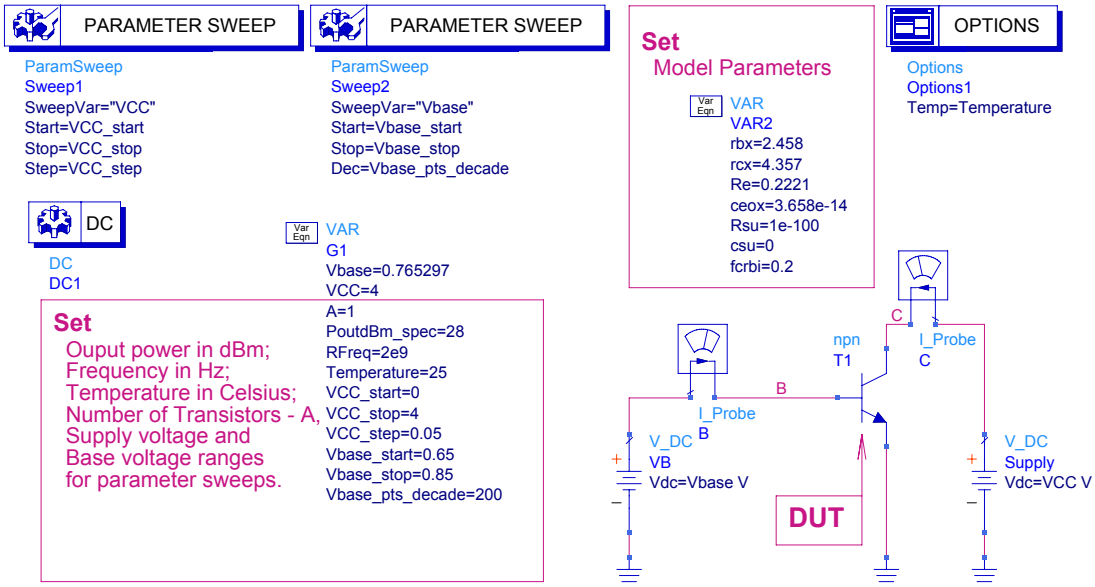


Figure 4.13: Test bench to design the bipolar power amplifier.

The variables are:

- A is the number of transistors in parallel.
- $PoutdBm\_spec$ is the required output power.
- $RFreq$ is the operating frequency.
- $Temperature$ is the operating temperature.
- VCC_start, VCC_stop, VCC_step are the start, stop and step values for the collector voltage sweep.
- $Vbase\_start$, $Vbase\_stop$, $Vbase\_pts\_decade$ are the start, stop and points per decade values for the gate voltage sweep.

The simplified HICUM/Level2 Large-Signal equivalent circuit in common emitter configuration with emitter and substrate connected together is shown in Fig. 4.14.

The I-V output characteristics of the bipolar transistor is shown in Fig. 4.15. Similar to the CMOS case, marker $m1$ determines the supply voltage V_{dc} and the

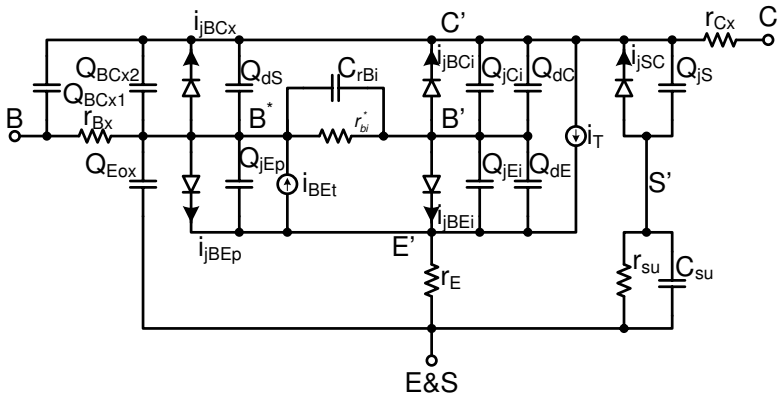


Figure 4.14: Simplified HICUM/Level2 large-signal equivalent circuit in common emitter configuration with emitter and substrate connected together.

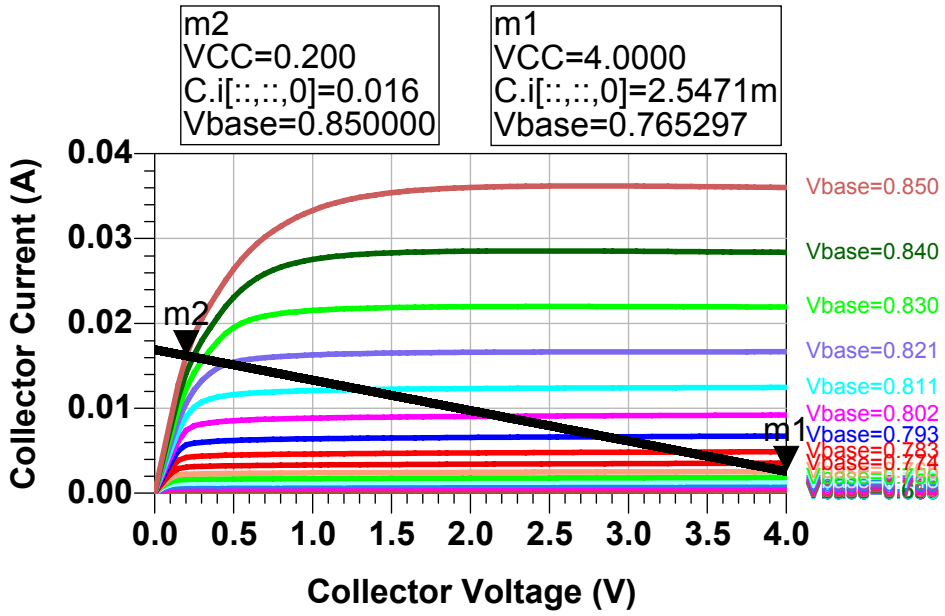


Figure 4.15: Bipolar output characteristics showing the choice of the operating point and load line.

output quiescent current I_{Out_Q}; and marker $m2$ determines the maximum output current I_{Out_max} and the amplitude of the output voltage $V_{Out} = V_{m1} - V_{m2}$.

Rewriting equation for I_{Out_Q} from (2.31) here

$$I_{Out\_Q} = -\frac{I_{Out\_max}\cos(\alpha/2)}{1-\cos(\alpha/2)} \tag{4.18}$$

and solving for α gives:

$$\alpha = 2\arccos\left(\frac{I_{Out\_Q}}{I_{Out\_Q} - I_{Out\_max}}\right) \tag{4.19}$$

For convenience, let's rewrite (2.35) and (2.36) here again

$$I_{dc}(\alpha) = \begin{cases} \frac{I_{Out\_max}}{2\pi}\frac{2\sin(\alpha/2)-\alpha\cos(\alpha/2)}{1-\cos(\alpha/2)} & I_{Out\_max} - 2I_Q \geq 0 \\ I_Q & I_{Out\_max} - 2I_Q < 0 \end{cases} \tag{4.20}$$

$$I_{Out} = I_1(\alpha) = \begin{cases} \frac{I_{Out\_max}}{2\pi}\frac{\alpha-\sin(\alpha)}{1-\cos(\alpha/2)} & I_{Out\_max} - 2I_{Out\_Q} \geq 0 \\ I_{Out\_max} - I_{Out\_Q} & I_{Out\_max} - 2I_{Out\_Q} < 0 \end{cases} \tag{4.21}$$

The small-signal equivalent circuit of the power amplifier is shown in Fig. 4.16.

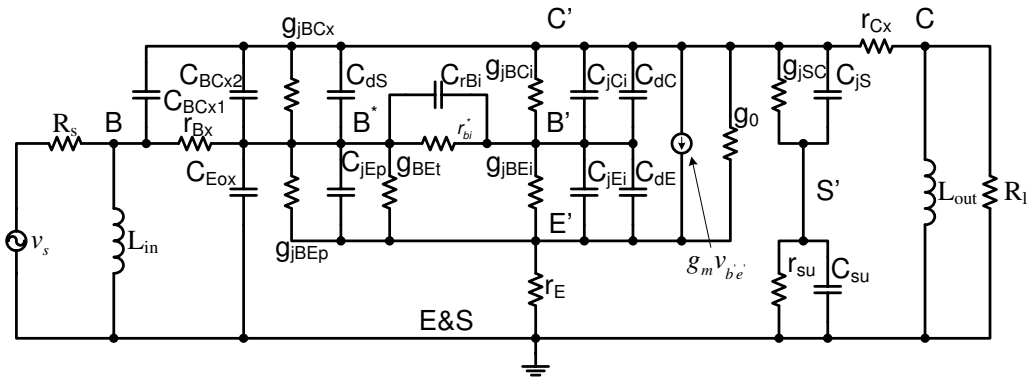


Figure 4.16: Small-signal equivalent circuit of the bipolar power amplifier.

Let's combine the components of the equivalent circuit shown in Fig 4.16 in the following way:

$$Z1 = \frac{1}{g_{jBEi} + j\omega(C_{jEi} + C_{dE})} \tag{4.22}$$

$$Z2 = \frac{1}{1/r_{bi} + j\omega C_{rBi}} \tag{4.23}$$

$$Z3 = \frac{1}{g_{jBEt} + g_{jBEp} + j\omega C_{jEp}} \tag{4.24}$$

$$Z4 = \frac{1}{j\omega C_{Eox}} \tag{4.25}$$

$$Z5 = r_{Bx} \tag{4.26}$$

$$Z_{mu1} = \frac{1}{g_{jBCi} + j\omega(C_{jC} + C_{dC})} \tag{4.27}$$

$$Z_{mu2} = \frac{1}{g_{jBCx} + j\omega(C_{Bcx2} + C_{dS})} \tag{4.28}$$

$$Z_{mu3} = \frac{1}{j\omega C_{Bcx1}} \tag{4.29}$$

$$Z_{o2} = \frac{1}{1/r_{su} + j\omega C_{su}} + \frac{1}{g_{jSC} + j\omega C_{jS}} \tag{4.30}$$

Additionally, the output inductance L_{out} at the node C is changed by the output inductance L_{out2} at the node C', the load resistance R_l is changed by R_{l2} and output conductance g_0 is placed between C' and ground instead of E' (see Fig. 4.17).

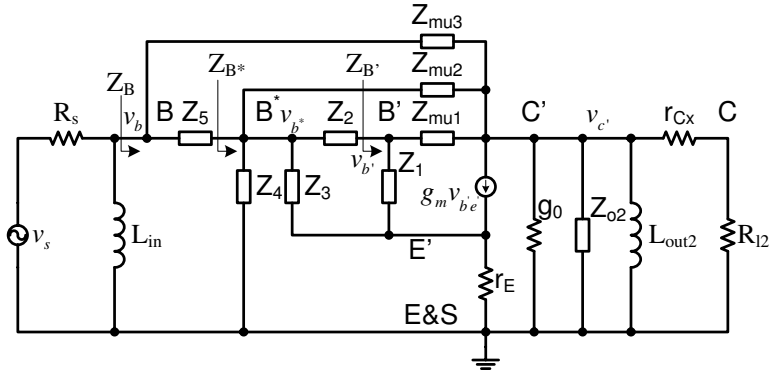


Figure 4.17: Small-signal equivalent circuit of the bipolar power amplifier, series and parallel connected elements are combined into the Z components.

The load resistance R_{l2} defined by the load line (see Fig. 4.15), neglecting influence of the feedback components Z_{mu1}, Z_{mu2} and Z_{mu3}, equals

$$R_{l2} = \begin{cases} \frac{V_{Out}}{I_{Out} - V_{Out}[g_o + \Re(1/Z_{o2})]} - r_{Cx} & \left(r_{Cx} || \frac{1}{g_o} || \Re(Z_{o2}) < \frac{V_{Out}}{I_{Out}} < \frac{1}{g_o + \Re(1/Z_{o2})}\right) \,\&\&\, (I_{Out\_max} - I_Q \geq 0) \\ do\ not\ consider & else \end{cases} \tag{4.31}$$

The Miller's theorem is applied to split the feedback components and emitter resistance (see Fig. 4.17) onto the input and output components (see Fig. 4.18). All steps required to perform this transformation are listed below:

$$ssg1 = \frac{v_{c'}}{v_{b'}} = -\frac{g_m \frac{1}{(1/r_{Cx} + R_{l2}) + \Re(1/Z_{o2}) + g_o}}{1 + r_E(1/Z_1 + g_m)} \tag{4.32}$$

$$Z_{mu1pi} = \frac{Z_{mu1}}{1 - ssg1} \tag{4.33}$$

$$Z_{mu1o} = \frac{Z_{mu1}}{1 - 1/ssg1} \tag{4.34}$$

$$Z_{e1} = r_e(1 + Z_1 g_m) \tag{4.35}$$

$$Z_{e3} = r_e \left(1 + \frac{Z_3 g_m}{Z_2/Z_1 + Z_2(Z_{e1} + Z_1)/\left(Z_{mu1pi} Z_1\right) + 1}\right) \tag{4.36}$$

$$Z_{B'} = \frac{Z_{mu1pi}(Z_1 + Z_{e1})}{Z_1 + Z_{e1} + Z_{mu1pi}} \tag{4.37}$$

$$ssg2 = \frac{v_{c'}}{v_{b^*}} = ssg1 \frac{Z_{B'}}{Z_2 + Z_{B'}} \tag{4.38}$$

$$Z_{mu2pi} = \frac{Z_{mu2}}{1 - ssg2} \tag{4.39}$$

$$Z_{mu2o} = \frac{Z_{mu2}}{1 - 1/ssg2} \tag{4.40}$$

$$Z_{B^*} = \frac{1}{1/\left(Z_{B'} + Z_2\right) + 1/\left(Z_3 + Z_{e3}\right) + 1/Z_4 + 1/Z_{mu2pi}} \tag{4.41}$$

$$ssg3 = \frac{v_{c'}}{v_b} = ssg2 \frac{Z_{B^*}}{Z_5 + Z_{B^*}} \tag{4.42}$$

$$Z_{mu3pi} = \frac{Z_{mu3}}{1 - ssg3} \tag{4.43}$$

$$Z_{mu3o} = \frac{Z_{mu3}}{1 - 1/ssg3} \tag{4.44}$$

where ssg1, ssg2 and ssg2 are small-signal gains.

Now, when the input and output nodes are separated the input (Z_B) and output (Z_o) impedances can be calculated as:

$$Z_B = \frac{1}{1/\left(Z_{B^*} + Z_5\right) + 1/Z_{mu3pi}} \tag{4.45}$$

and

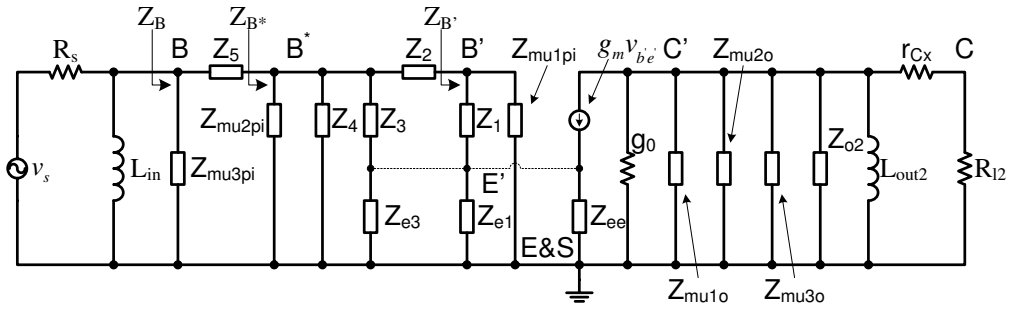


Figure 4.18: Small-signal equivalent circuit of the power amplifier, applying of the Miller's theorem.

$$Z_o = \frac{1}{1/Z_{o2} + 1/Z_{mu1o} + 1/Z_{mu2o} + 1/Z_{mu3o} + g_o} \tag{4.46}$$

Then, the output inductance (L_{out2}) equals:

$$L_{out2} = \frac{1}{\omega \Im(1/Z_o)} \tag{4.47}$$

Conjugate matched theory is used to find the input inductance L_{in} and source resistance R_s:

$$L_{in} = \frac{1}{\omega \Im(1/Z_B)} \tag{4.48}$$

and

$$R_s = \frac{1}{\Re(1/Z_B)} \tag{4.49}$$

The last unknown components in Fig. 4.16 are R_l and L_{out} which can be expressed as:

$$R_l = \frac{R_{cx}^4 + 2R_{l2}R_{cx}^3 + \omega^2 L_{out2}^2 R_{l2}^2 + R_{l2}^2 R_{cx}^2}{-R_{cx}^3 - 2R_{cx}^2 R_{l2} - R_{l2}^2 R_{cx} + \omega^2 L_{out2}^2 R_{l2}} \tag{4.50}$$

and

$$L_{out} = \frac{R_{cx}^4 + 2R_{l2}R_{cx}^3 + \omega^2 L_{out2}^2 R_{l2}^2 + R_{l2}^2 R_{cx}^2}{\omega^2 L_{out2}(R_{l2}^2 + 2R_{l2}R_{cx} + R_{cx}^2)} \tag{4.51}$$

The output power is defined as:

$$P_{Out} = \frac{\left|\frac{V_{Out}/[1/R_l+1/(j\omega L_{out})]}{r_{Cx}+1/[1/R_l+1/(j\omega L_{out})]}\right|^2}{2R_l} = \frac{\left|\frac{V_{Out}}{r_{Cx}[1/R_l+1/(j\omega L_{out})]+1}\right|^2}{2R_l} \tag{4.52}$$

where V_{Out} is an amplitude of the output voltage $(V_{m1} - V_{m2})$ and R_l is expressed in (4.50).

Estimated output power for different output voltages (load lines) and bias currents is shown in Fig. 4.19.

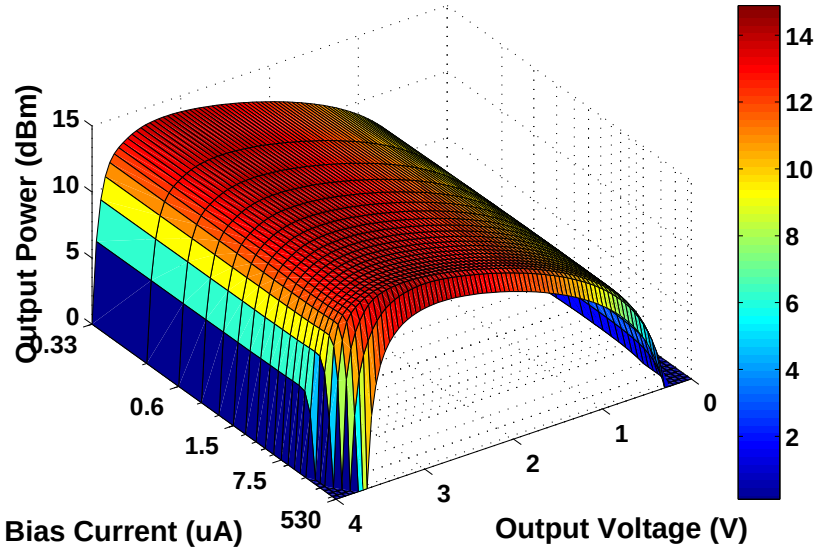


Figure 4.19: Expected output power based on the analysis of the bipolar output characteristics as a function of the chosen operating point and load line.

The collector efficiency is given by:

$$\eta = \frac{P_{Out}}{V_{dc}I_{dc}} \tag{4.53}$$

where V_{dc} equals $V_{m1} + I_{dc}r_{Cx}$

The collector efficiency is shown in Fig. 4.20.

In the same way as for the CMOS design guide, the small-signal transducer power gain with compression coefficient g_c is used to estimate the power added efficiency:

$$pae = \eta\left(1 - \frac{1}{g_t}\right) \tag{4.54}$$

where

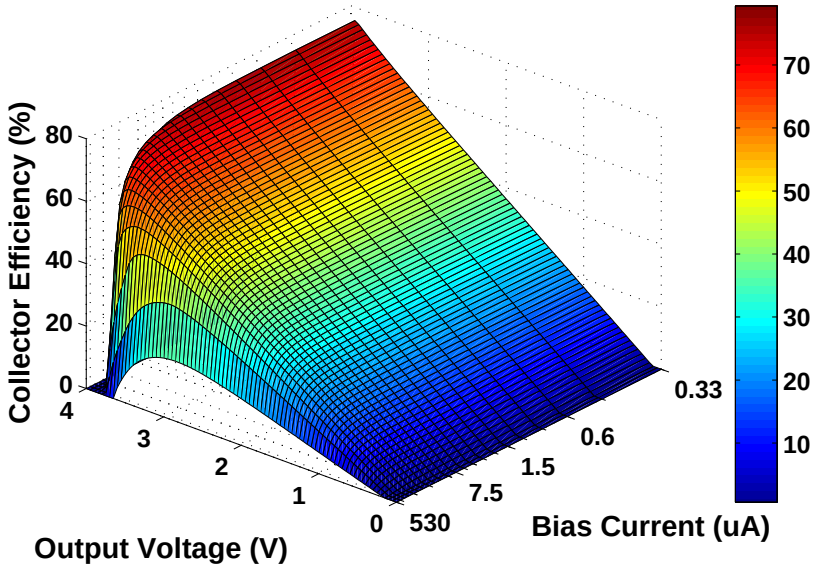


Figure 4.20: Expected collector efficiency based on the analysis of the bipolar output characteristics as a function of the chosen operating point and load line.

$$g_t = g_c \frac{p_{out}}{p_{in}} = g_c \frac{R_s}{R_l} \left| \frac{ssg3}{r_{Cx}\left[1/R_l + 1/\left(j\omega L_{out}\right)\right] + 1} \right| \tag{4.55}$$

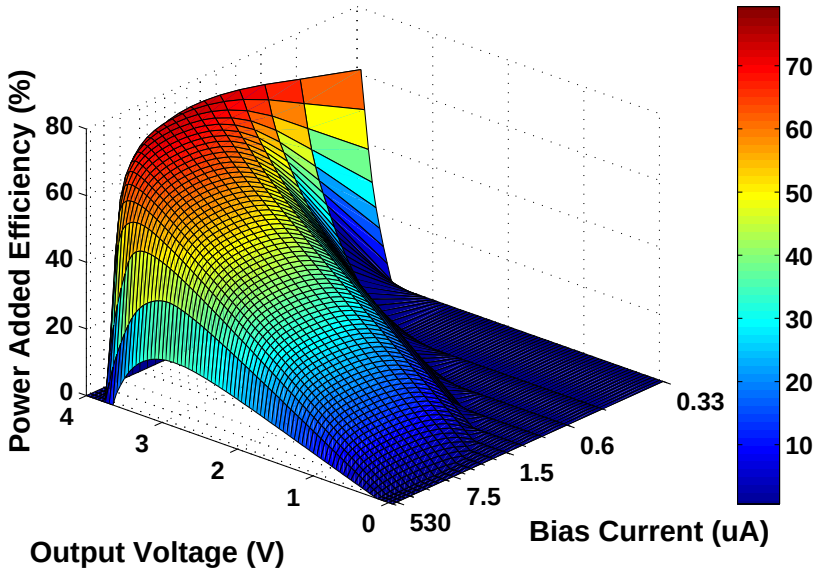


Figure 4.21: Estimated power added efficiency based on the analysis of the bipolar output characteristics as a function of the chosen operating point and load line.

Fig. 4.21 shows predicted values of the power added efficiency for the set of the

bias and output voltages.

As an example, the bias voltage of 0.765 V (bias current of 28.4 μA) and the output voltage of 3.8 V corresponds to the power added efficiency of 67.5 % with the output power of 11.9 dBm and collector efficiency of 67.6 %. Similar to the CMOS design guide the output power can be adjusted as follow

$$A = A \cdot Round\left(\frac{P_{Out\_spec}}{P_{Out}}\right) \tag{4.56}$$

The estimated components values for the example given above (source resistance of 118 Ω, input inductance of 1.7 nH, output inductance of 73.1 nH and load resistance of 456 Ω) are substituted in the harmonic balance test bench (see Fig. 4.22) to simulate the large-signal behaviour of the power amplifier prototype.

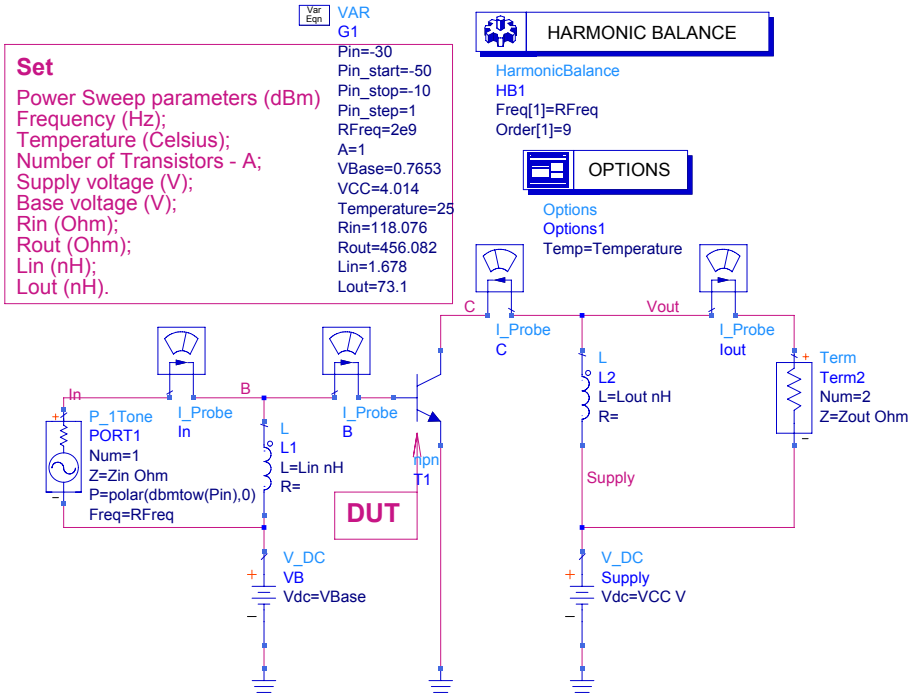


Figure 4.22: Harmonic balance test bench to design the bipolar power amplifier.

The large-signal analysis of the bipolar power amplifier prototype shows that the saturated output power of 12 dBm (m1), collector efficiency of 65 % (m2) and power added efficiency of 64.7 %) (m3) (see Fig. 4.23) are in a good agreement with the predicted one (output power of 11.9 dBm, collector efficiency of 67.6 % and power added efficiency of 67.5 %).

The time domain waveforms of the collector voltage and transfer current (current from the current source in the model) for different values of the input power are

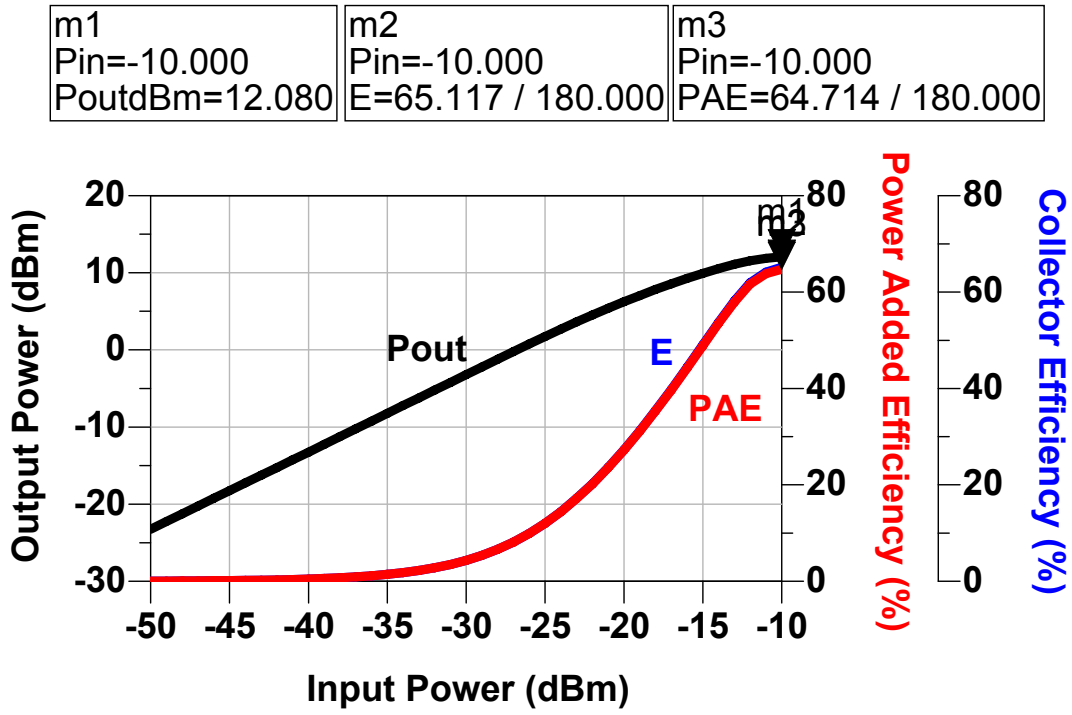


Figure 4.23: Output power, efficiency and power added efficiency as a function of the input power.

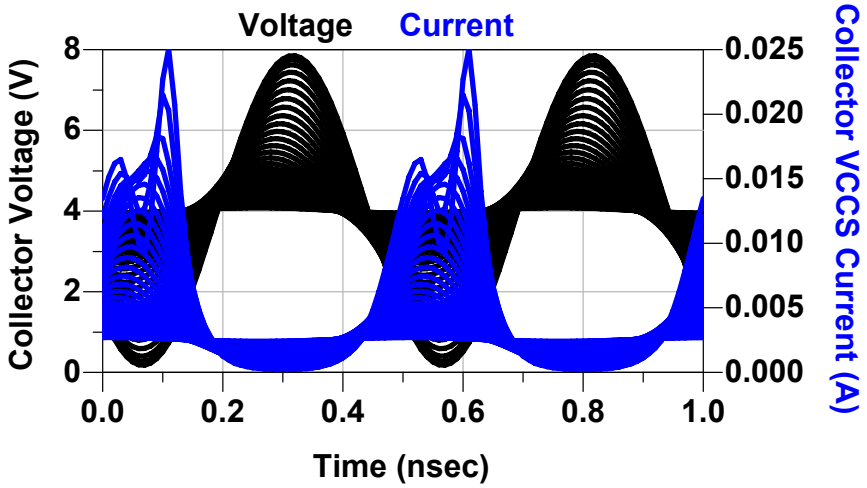


Figure 4.24: Collector voltage and transfer current waveforms of the designed bipolar power amplifier prototype.

shown in Fig. 4.24. Higher values of the input power cause bifurcated pulses of the transfer current waveform.

Fig. 4.25 shows the dynamic load lines for different values of input power which

are located lengthways the chosen load line at the output characteristics (see Fig. 4.15).

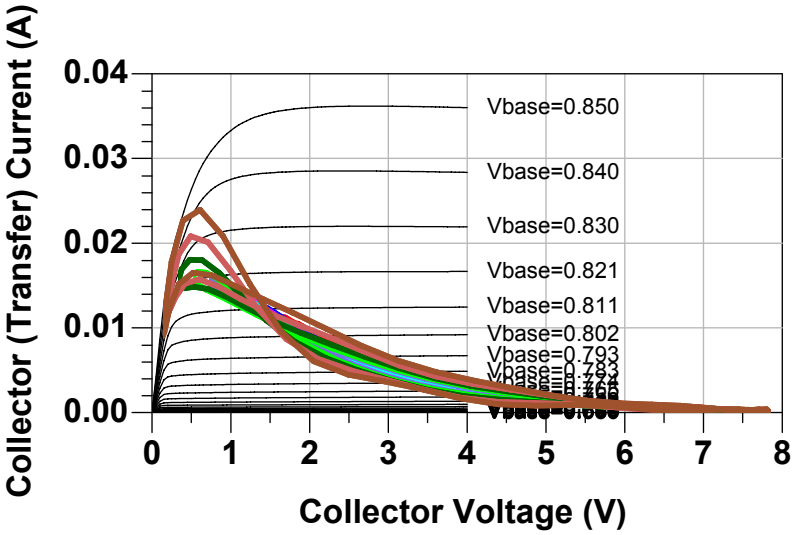


Figure 4.25: Large-signal simulation of the bipolar power amplifier prototype, showing dependence of the dynamic load line on the input power.

4.2 Load-Pull Analysis

The load-pull is a well known technique over the last three decades. It's also found itself in the power amplifier design. The outcomes of this techniques are a graphical representation of the interested parameters versus source or load impedances. For the power amplifier design such parameters are the output power, drain(collector) efficiency, power added efficiency, gain and input impedance and the variables are the device size, supply voltage, operating point, input power, and load impedance. The load impedance is usually meant by the impedance at fundamental harmonic but also could be expanded for the higher harmonics. The typical load-pull setup consists of a device under test, source, load and two impedance tuners (see Fig. 4.26).

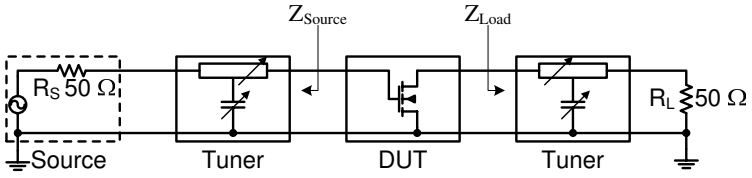


Figure 4.26: Load-pull setup.

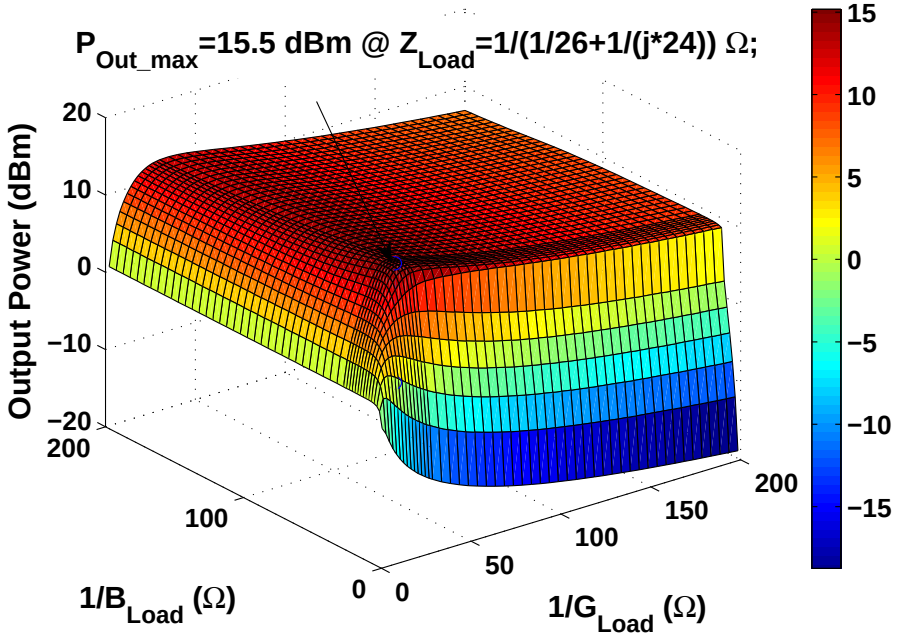


Figure 4.27: Output power of the designed CMOS prototype power amplifier as a function of load impedance at the fundamental harmonic.

It's clear that the pure load-pull techniques is a time consuming procedure which has multidimensional matrixes of the solutions at the output. Consequently, ap-

plying this technique at the prototype which is build previously when the transistor size, supply voltage, operating point, input power and load impedance are predefined leads to a significant reduce of the computation time.

The results of the load-pull simulation of the CMOS power amplifier prototype with the input power of 0 dBm are shown in Fig. 4.27 (Output power), Fig. 4.28 (Drain efficiency) and Fig. 4.29 (Power added efficiency), where $Z_{Load} = 1/(G_{Load} + jB_{Load})$. Fig. 4.27 shows that the power amplifier is able to achieve the output power of 15.45 dBm at the output impedance of $11.96 + j12.96\ \Omega$. The highest drain efficiency of 72.3 % occurs at the output impedance of $64.5 + j57.1\ \Omega$ and the output impedance of $56.6 + j40.1\ \Omega$ gives the peak value of the power added efficiency of 67.5 %.

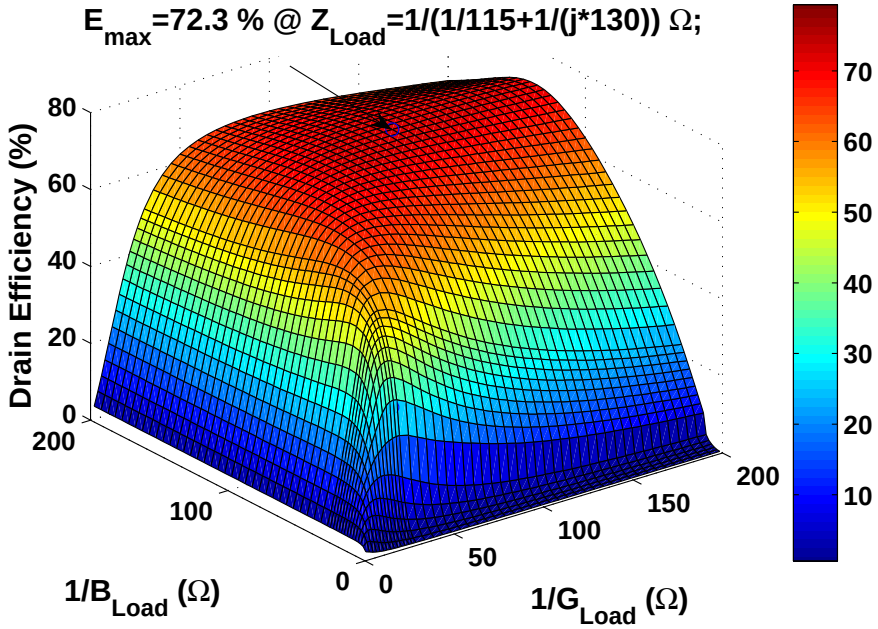


Figure 4.28: Drain efficiency of the designed CMOS prototype power amplifier as a function of load impedance at the fundamental harmonic.

Table 4.1 makes the comparison of the CMOS power amplifier prototype performance at each step of the design procedure (analytical analysis, large-signal simulation at the saturation and load-pull analysis).

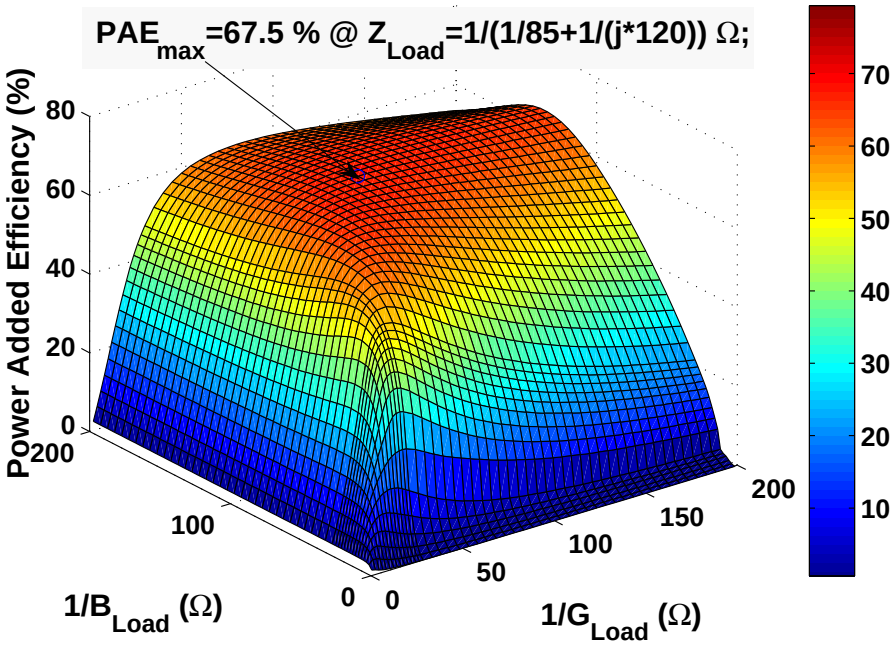


Figure 4.29: Power added efficiency of the designed CMOS prototype power amplifier as a function of load impedance at the fundamental harmonic.

Table 4.1: Summary table, showing the analytically estimated and simulated performances of the CMOS prototype power amplifier.

	Analytical Analysis	**Large-signal Simulation**	**Load-pull Analysis**	
Transistor Type	NANA	NANA	NANA	
Gate Fingers Connection	one side	one side	one side	
Length	0.4	0.4	0.4	μm
Width	1000	1000	1000	μm
Number of Fingers	40	40	40	
Supply Voltage	1.65	1.65	1.65	V
Bias Voltage	0.4	0.4	0.4	V
Input Power	N/A	0	-0.67	dBm
Output Impedance	$54.7 + j43.2$	$54.7 + j43.2$	$56.6 + j40.1$	Ω
Source Impedance	$5.2 + j34.5$	$5.2 + j34.5$	$6.2 + j30$	Ω
Output Power	11.59	11.56	11.5	dBm
Drain Efficiency	70.7	71.79	71.9	%
Power Added Efficiency	65.7	66.78	67.5	%

4.3 Transformer-Based Matching Network Design

There exists a lot of matching network configurations all of them has some advantages and drawbacks which has to be considered to make the right choice. The analytical analysis of the matching network help to make a fast estimation of the required components and to predict its loss. This part gives a derivation of the equation set for the transformer-based matching network.

The matching network could include "parasitic" components such as bond wires, bond pads and parasitic capacitors.

4.3.1 Analysis of Bond Wires

The aim of the analysis presented here is to give the analytical equations for the series inductance and series resistance of the bond wire connection (see Fig. 4.30).

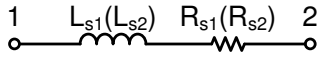


Figure 4.30: Typical RF lumped model of the bond wire connection.

Fig. 4.31 shows the solid model used for analytical analysis. It consists of the bond wires and their images in accordance with the theory of "current images" which are approximated by the three strait filaments. The one bond wire and two bond wires systems are considered.

The component values of inductance (L_{s1}) and resistance (R_{s1}) [March 91] for the single bond wire are given by:

$$\begin{aligned} L_{s1} = L_1 + L_2 + L_3 \quad &- \quad 2M_{12} - 2M_{23} - 2M_{13} \\ &- \quad M_{11im} - M_{12im} - M_{13im} \\ &- \quad M_{21im} - M_{23im} - M_{22im} \\ &- \quad M_{31im} - M_{32im} - M_{33im} \end{aligned} \tag{4.57}$$

and

$$R_{s1} = \begin{cases} R_{dc} \cosh\left[0.041(\frac{d}{d_s})^2\right] & \frac{d}{d_s} \leq 3.394 \\ R_{dc}\left(0.25\frac{d}{d_s} + 0.2654\right) & \frac{d}{d_s} \geq 3.394 \end{cases} \tag{4.58}$$

where L is a self inductance of the strait filaments; M is a mutual inductances between strait filaments; $R_{dc} = 4\rho l/(\pi d^2)$ is a dc resistance of the bond wire; d is

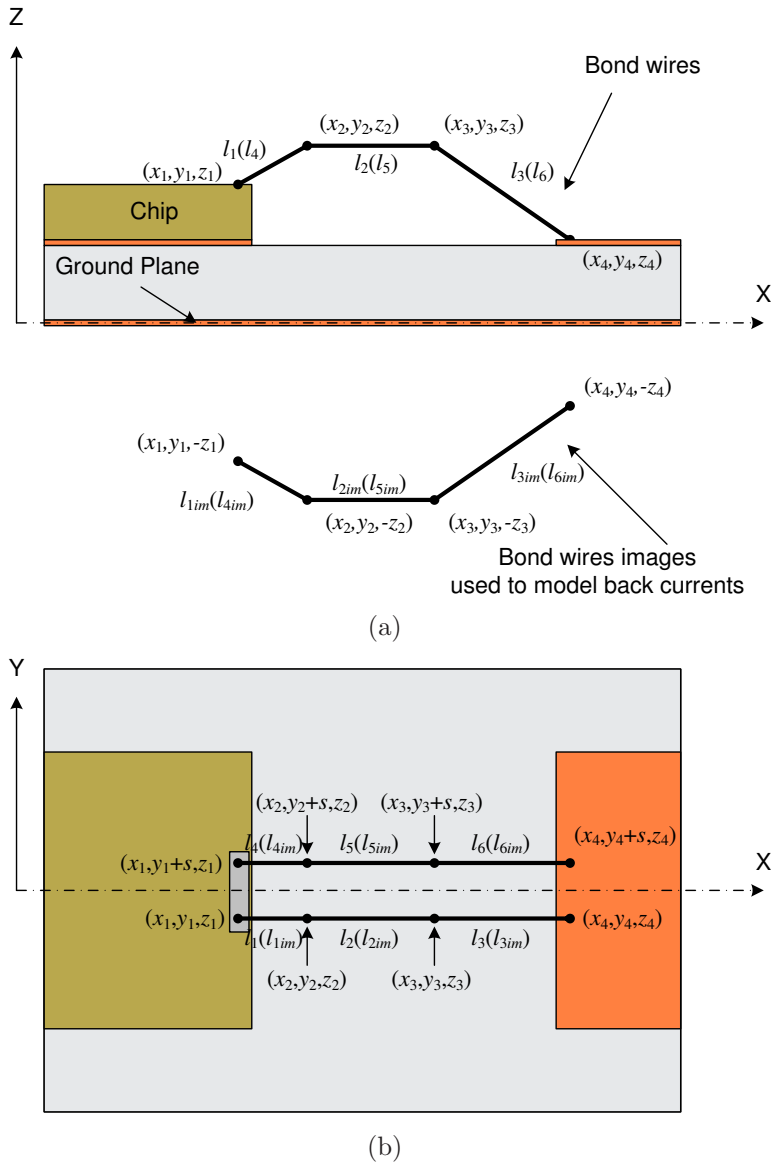


Figure 4.31: Solid model used for the analytical analysis of the bond wire connection.: (a) Front view; (b) Top view.

a diameter of the bond wire; and d_s is a skin depth of the bond wire material at given frequency:

$$d_s = \sqrt{\frac{\rho}{\pi f \mu_0 \mu_r}} \tag{4.59}$$

where ρ is resistivity of the bond wire material ($2.62 \cdot 10^{-8}\ \Omega \cdot m$ for aluminium); and f is frequency (Hz).

In case of two parallel bond wires the inductance (L_{s2}) and resistance (R_{s2}) are given by:

$$L_{s2} = \frac{L_{s1}}{2} + \frac{M_{14} - M_{14im} + M_{15} - M_{15im} + M_{16} - M_{16im}}{2} + \frac{M_{24} - M_{24im} + M_{25} - M_{25im} + M_{26} - M_{26im}}{2} + \frac{M_{34} - M_{34im} + M_{35} - M_{35im} + M_{36} - M_{36im}}{2} \quad (4.60)$$

and

$$R_{s2} = \frac{F_p R_{s1}}{2} \quad (4.61)$$

where F_p is the proximity factor [March 91]:

$$F_p = 1 + 0.8478 \exp[-0.9435(s/d)] \quad (4.62)$$

The self inductances in (4.57) and (4.61) can be expressed by the inductance of a strait wire positioned horizontally at infinite distance above ground [March 91]:

$$L = \frac{\mu_0 l}{2\pi} \left\{ \ln \left[\frac{4l}{d} + \sqrt{1 + \left(\frac{2l}{d}\right)^2} \right] + \frac{d}{2l} - \sqrt{1 + \left(\frac{d}{2l}\right)^2} + \mu_r \delta \right\} \quad (4.63)$$

where μ_0 is permeability of free space ($4\pi \cdot 10^{-7} H/m$); μ_r is relative permeability of the bond wire material; l is a length of the bond wire; d is a diameter of the bond wire; δ is a skin effect factor.

The skin effect factor was introduced to take care about a high frequency effect and equals:

$$\delta = 0.25 \tanh(4 d_s/d) \quad (4.64)$$

where d_s is a skin depth of the bond wire material at given frequency.

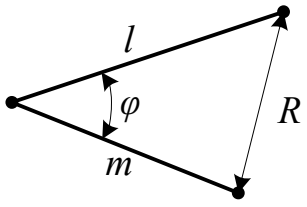


Figure 4.32: Unequal filaments meeting at a point.

The mutual inductances M_{12} between l_1 and l_2; M_{23} between l_2 and l_3 in (4.60) and (4.57) are expressed by the mutual inductance between two unequal filaments meeting at a point (see Fig. 4.32) [Grover 46]:

$$M = \frac{\mu_0}{2\pi} \cos\varphi \left(l \tanh^{-1} \frac{m}{l+R} + m \tanh^{-1} \frac{l}{m+R} \right) \tag{4.65}$$

$$\cos\varphi = \frac{l^2 + m^2 - R^2}{2lm} \tag{4.66}$$

where l and m are the length of the filaments; φ is the angle between filaments; and R is the distance between their ends.

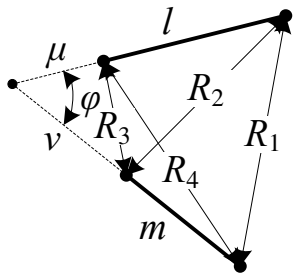


Figure 4.33: Unequal filaments in the sam plane, not meeting.

The mutual inductances M_{13} between l_1 and l_3; M_{11im} between l_1 and l_{11im}; M_{12im} between l_1 and l_{12im}; M_{13im} between l_1 and l_{13im}; M_{21im} between l_2 and l_{11im}; M_{22im} between l_2 and l_{12im}; M_{23im} between l_2 and l_{13im}; M_{31im} between l_3 and l_{11im}; M_{32im} between l_3 and l_{12im}; M_{33im} between l_3 and l_{13im} are represented by the mutual inductances between two unequal filaments in the same plane, not meeting (see Fig. 4.33) [Grover 46]:

$$\begin{aligned} M &= \frac{\mu_0}{2\pi} \cos\varphi \left[(\mu + l) \tanh^{-1} \frac{m}{R_1 + R_2} + (\nu + m) \tanh^{-1} \frac{l}{R_1 + R_4} \right. \\ &- \left. \mu \tanh^{-1} \frac{m}{R_3 + R_4} - \nu \tanh^{-1} \frac{l}{R_2 + R_3} \right] \end{aligned} \tag{4.67}$$

$$\cos\varphi = \frac{\alpha^2}{2lm} \tag{4.68}$$

where $\alpha^2 = R_4^2 - R_3^2 + R_2^2 - R_1^2$; l and m are the length of the filaments; R_1, R_2, R_3, and $R4$ are the distances between the ends of the filaments as shown in Fig. 4.33; and lengths μ and ν are given by:

$$\mu = \frac{\left[2m^2 \left(R_2^2 - R_3^2 - l^2\right) + \alpha^2 \left(R_4^2 - R_3^2 - m^2\right)\right] l}{4l^2m^2 - a^4} \tag{4.69}$$

$$\nu = \frac{\left[2l^2\left(R_4^2 - R_3^2 - m^2\right) + \alpha^2\left(R_2^2 - R_3^2 - l^2\right)\right] m}{4l^2m^2 - a^4} \tag{4.70}$$

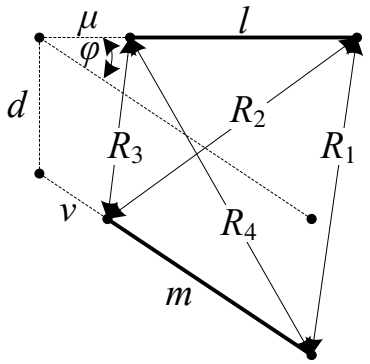


Figure 4.34: Mutual inductance of two straight filaments placed in any desired positions.

The mutual inductances M_{14im} between l_1 and l_{4im}; M_{15} between l_1 and l_5; M_{15im} between l_1 and l_{5im}; M_{16} between l_1 and l_6; M_{16im} between is l_1 and l_{6im}; M_{24} between l_2 and l_4; M_{24im} between l_2 and l_{4im}; M_{25im} between l_2 and l_{5im}; M_{26} between l_2 and l_6; M_{26im} between l_2 and l_{6im}; M_{34} between l_3 and l_4; M_{34im} between l_3 and l_{4im}; M_{35} between l_3 and l_5; M_{35im} is between l_3 and l_{5im}; M_{36im} between l_3 and l_{6im} are represented by the mutual inductance of two straight filaments placed in any desired positions (see Fig. 4.34) [Grover 46]:

$$\begin{aligned} M &= \frac{\mu_0}{2\pi}\cos\varphi\left[(\mu+l)\tanh^{-1}\frac{m}{R_1+R_2} + (\nu+m)\tanh^{-1}\frac{l}{R_1+R_4}\right. \\ &- \left.\mu\tanh^{-1}\frac{m}{R_3+R_4} - \nu\tanh^{-1}\frac{l}{R_2+R_3}\right] - \frac{\Omega d}{\sin\varphi} \end{aligned} \tag{4.71}$$

$$\begin{aligned} \Omega &= \tan^{-1}\left[\frac{d^2\cos\varphi + (\mu+l)(\nu+m)\sin^2\varphi}{dR_1\sin\varphi}\right] \\ &- \tan^{-1}\left[\frac{d^2\cos\varphi + (\mu+l)\nu\sin^2\varphi}{dR_2\sin\varphi}\right] \\ &+ \tan^{-1}\left[\frac{d^2\cos\varphi + \mu\nu\sin^2\varphi}{dR_3\sin\varphi}\right] \\ &- \tan^{-1}\left[\frac{d^2\cos\varphi + \mu(\nu+m)\sin^2\varphi}{dR_4\sin\varphi}\right] \end{aligned} \tag{4.72}$$

$$\cos\varphi = \frac{\alpha^2}{2lm} \tag{4.73}$$

where $\alpha^2 = R_4^2 - R_3^2 + R_2^2 - R_1^2$; $d^2 = R_3^2 - \mu^2 - \nu^2 + 2\mu\nu\cos\varphi$; φ is the angle between the filament l and intersection line which is produced by the planes which are passed through through the filaments l and m in such a way as to intersect at right angles; and lengths μ and ν are given by:

$$\mu = \frac{\left[2m^2\left(R_2^2 - R_3^2 - l^2\right) + \alpha^2\left(R_4^2 - R_3^2 - m^2\right)\right] l}{4l^2m^2 - a^4} \tag{4.74}$$

$$\nu = \frac{\left[2l^2\left(R_4^2 - R_3^2 - m^2\right) + \alpha^2\left(R_2^2 - R_3^2 - l^2\right)\right] m}{4l^2m^2 - a^4} \tag{4.75}$$

The mutual inductances M_{14} between l_1 and l_4; M_{25} between l_2 and l_5; M_{36} between l_3 and l_6 are represented by the mutual inductance of two equal parallel straight filaments [Grover 46]:

$$M = \frac{\mu_0}{2\pi} l \left[log\frac{l}{s} + \sqrt{1 + \frac{l^2}{s^2}} - \sqrt{1 + \frac{s^2}{l^2}} + \frac{s}{l} \right] \tag{4.76}$$

where l is the length of filaments; and s is the distance between them.

Table 4.2 contains the bond wire coordinates which approximate typical bond wires used during this work for connecting of the input (one bond wire) and output (two bond wires with 50 μm pitch) pads.

Table 4.2: Bond wires coordinates for analytical analysis.

Points	**Bond Wire 1**			**Bond Wire 2**			
	X	Y	Z	X	Y	Z	
1	0	0	700	0	50	700	μm
2	84	0	800	84	50	800	μm
3	250	0	800	250	50	800	μm
4	500	0	500	500	50	500	μm

Components of the equivalent circuit (series resistance and inductance) for bond wires which shape is described in Table 4.2 are calculated and shown in Fig. 4.35.

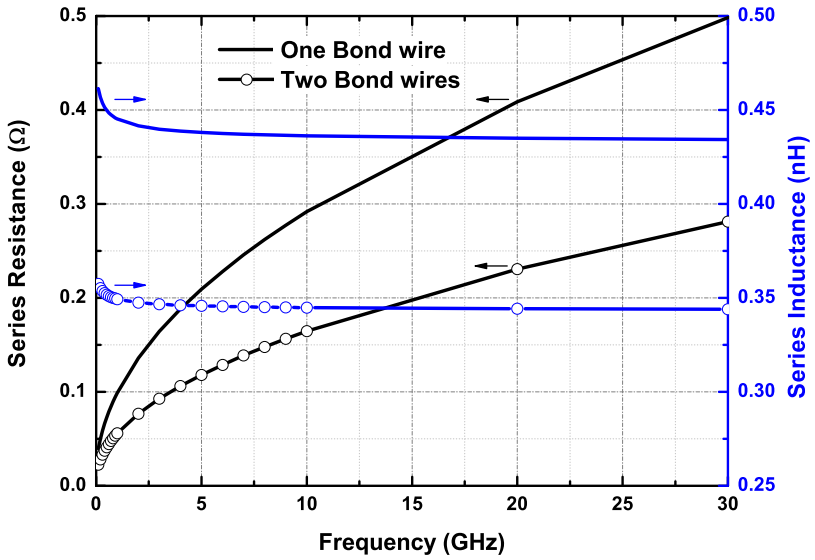


Figure 4.35: Frequency behaviour of analytically estimated series resistance and series inductance of typical bond wire configurations: one bond wire and two parallel bond wires with a pitch of 50 μm.

4.3.2 Analysis of Transformer as Matching Network

Transformers are produced in different technologies and have different configurations (metal stack, winding scheme etc.) but all of them can be described by inductance of the windings, quality factor of the windings and coupling coefficients between them.

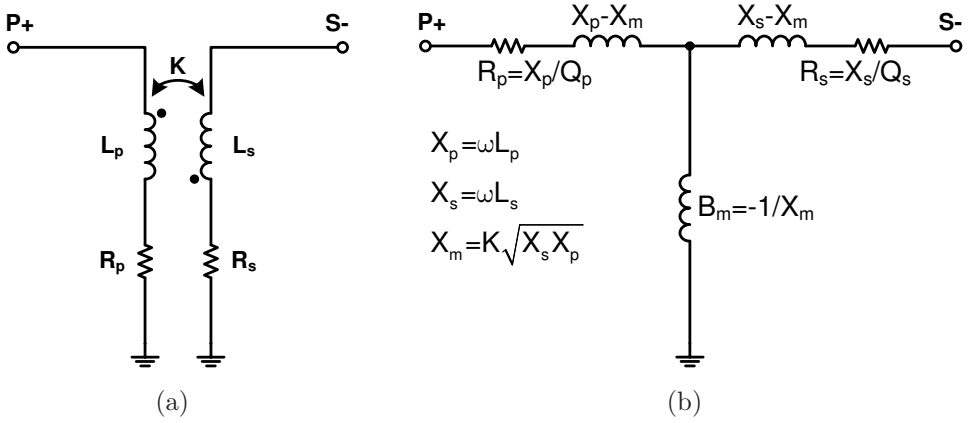


Figure 4.36: Transformer: (a) Lumped model; (b) Equivalent T-model.

The simplified transformer model is shown in Fig. 4.36(a). The equivalent T-model (see Fig. 4.36(b)) is used here to perform analytical analysis of the transformer based matching network.

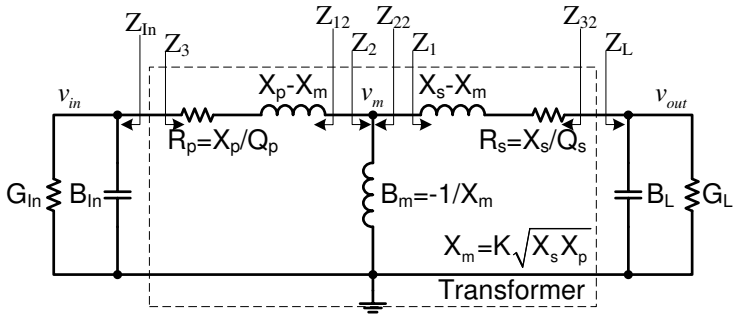


Figure 4.37: Transformer-based matching network.

Fig. 4.37 shows typical example of the transformer-based matching network. The matching network has to transform load admittance G_L into input admittance G_{In}. This circuit has seven unknowns such as load capacitive susceptance B_L, input capacitive susceptance B_{In}, inductive reactance of the primary winding X_p, inductive reactance of the secondary winding X_s, quality factor of the primary winding Q_p, quality factor of the secondary winding Q_s and coupling coefficient between them K that leads to unbounded solution sets. To overcome this uncertainty, the quality factors and coupling coefficient are treated as technology

and winding scheme limiting factors that leads to the reduction of the number of unknowns and unambiguous solution.

The conjugate matching theory is applied to formulate four equations to solve the system with four unknowns:

$$\begin{cases} G_3 = G_{In} \\ B_3 = -B_{In} \\ G_{32} = G_L \\ B_{32} = -B_L \end{cases} \tag{4.77}$$

Load impedance Z_L equals to $R_L + jX_L$ where

$$R_L = \frac{G_L}{G_L^2 + B_L^2} \tag{4.78}$$

and

$$X_L = -\frac{B_L}{G_L^2 + B_L^2} \tag{4.79}$$

Internal impedance Z_1 equals to $R_1 + jX_1$. Its components are expressed as

$$R_1 = R_L + R_s \tag{4.80}$$

and

$$X_1 = X_L + X_s - X_m \tag{4.81}$$

Transforming the impedance components R_1 and X_1 into the admittance components G_1 and B_1 gives:

$$G_1 = \frac{R_1}{R_1^2 + X_1^2} \tag{4.82}$$

and

$$B_1 = -\frac{X_1}{R_1^2 + X_1^2} \tag{4.83}$$

Admittance $Y_2 = G_2 + jB_2$ where G_2 and B_2 equal:

$$G_2 = G_1 \tag{4.84}$$

and

$$B_2 = B_1 + B_m \tag{4.85}$$

Then transformation of Y_2 into Z_2 gives:

$$R_2 = \frac{G_2}{G_2^2 + B_2^2} \tag{4.86}$$

and

$$X_2 = -\frac{B_2}{G_2^2 + B_2^2} \tag{4.87}$$

Components R_3 and X_3 of the internal impedance Z_3 are:

$$R_3 = R_2 + R_p \tag{4.88}$$

and

$$X_3 = X_2 + X_p - X_m \tag{4.89}$$

Finally G_3 and B_3 are expressed as:

$$G_3 = \frac{R_3}{R_3^2 + X_3^2} \tag{4.90}$$

and

$$B_3 = -\frac{X_3}{R_3^2 + X_3^2} \tag{4.91}$$

Performing the same operation from the left to the right the last two terms (G_{32} and B_{32}) in (4.77) can be found:

$$R_{In} = \frac{G_{In}}{G_{In}^2 + B_{In}^2} \tag{4.92}$$

$$X_{In} = -\frac{B_{In}}{G_{In}^2 + B_{In}^2} \tag{4.93}$$

$$R_{12} = R_{In} + R_p \tag{4.94}$$

$$X_{12} = X_{In} + X_p - X_m \tag{4.95}$$

$$G_{12} = \frac{R_{12}}{R_{12}^2 + X_{12}^2} \tag{4.96}$$

$$B_{12} = -\frac{X_{12}}{R_{12}^2 + X_{12}^2} \tag{4.97}$$

$$G_{22} = G_{12} \tag{4.98}$$

$$B_{22} = B_{12} + B_m \tag{4.99}$$

$$R_{22} = \frac{G_{22}}{G_{22}^2 + B_{22}^2} \tag{4.100}$$

$$X_{22} = -\frac{B_{22}}{G_{22}^2 + B_{22}^2} \tag{4.101}$$

$$R_{32} = R_{22} + R_s \tag{4.102}$$

$$X_{32} = X_{22} + X_s - X_m \tag{4.103}$$

$$G_{32} = \frac{R_{32}}{R_{32}^2 + X_{32}^2} \tag{4.104}$$

$$B_{32} = -\frac{X_{32}}{R_{32}^2 + X_{32}^2} \tag{4.105}$$

Substituting (4.90), (4.91), (4.104) and (4.105) in to (4.77) and solving it for X_s, B_L, X_p and B_{In} gives:

$$\begin{cases} X_s = \frac{Q_s\sqrt{K^2Q_pQ_s+1}}{G_L(1+K^2Q_pQ_s+Q_s^2)} \\ B_L = \frac{Q_sG_L}{\sqrt{K^2Q_pQ_s+1}} \\ X_p = \frac{Q_p\sqrt{K^2Q_pQ_s+1}}{G_{In}\left(1+K^2Q_pQ_s+Q_p^2\right)} \\ B_{In} = \frac{Q_pG_{In}}{\sqrt{K^2Q_pQ_s+1}} \end{cases} \tag{4.106}$$

Next step is to calculate the efficiency of the transformer matching network. Assumption that the matching network is driven by the current source on the left side in such way that $v_{in} = 1$ gives:

$$v_m = \frac{Z_2}{Z_3} \tag{4.107}$$

Then, the output voltage equals:

$$v_{out} = \frac{v_m Z_L}{Z_1} \tag{4.108}$$

Finally, the power delivered to the load is:

$$P_{out} = \frac{|v_{out}|^2 G_L}{2} \tag{4.109}$$

and power available from the source is:

$$P_{avs} = \frac{G_{In}}{2} \tag{4.110}$$

Then, the efficiency of the matching network when the input and output are simultaneously matched equals:

$$\begin{aligned} E &= \frac{P_{out}}{P_{avs}} \cdot 100 \Bigg|_{X_s=\frac{Q_s\sqrt{K^2Q_pQ_s+1}}{G_L(1+K^2Q_pQ_s+Q_s^2)}, B_L=\frac{Q_sG_L}{\sqrt{K^2Q_pQ_s+1}}} \\ &= \frac{Q_pQ_sK^2\sqrt{Q_pQ_sK^2+1}}{2Q_pQ_sK^2+Q_pQ_sK^2\sqrt{Q_pQ_sK^2+1}+2\sqrt{Q_pQ_sK^2+1}+2} \cdot 100 \\ &= \frac{1}{1+\frac{2}{Q_pQ_sK^2}+2\sqrt{\frac{1}{Q_pQ_sK^2}\left(1+\frac{1}{Q_pQ_sK^2}\right)}} \cdot 100 \end{aligned} \tag{4.111}$$

The same answer for E, using another approach, is derived in [Aoki 02,a].

Fig. 4.38 shows the efficiency of the transformer-based matching network for cases when the coupling coefficient equals 1 (see Fig. 4.38(a)), 0.8 (see Fig. 4.38(b)), 0.6 (see Fig. 4.38(c)), 0.4 (see Fig. 4.38(d)). Typical integrated transformers have the coupling coefficient in the range from 0.6 to 0.8 and the winding quality factor in the range from 5 to 15 so the expected efficiency of the transformer-based matching network is between 50 % (-3 dB) and 80 % (-1 dB).

The next step is to design the transformer with predicted parameters of Q_p, Q_s, K, L_p and L_s. The designed transformer requires a method to estimated its performance. The way how to do it is described below.

The definition of maximum transducer power gain [Gonzalez 97], under simultaneous conjugate match condition gives the minimum power loss of the transformer and is given by:

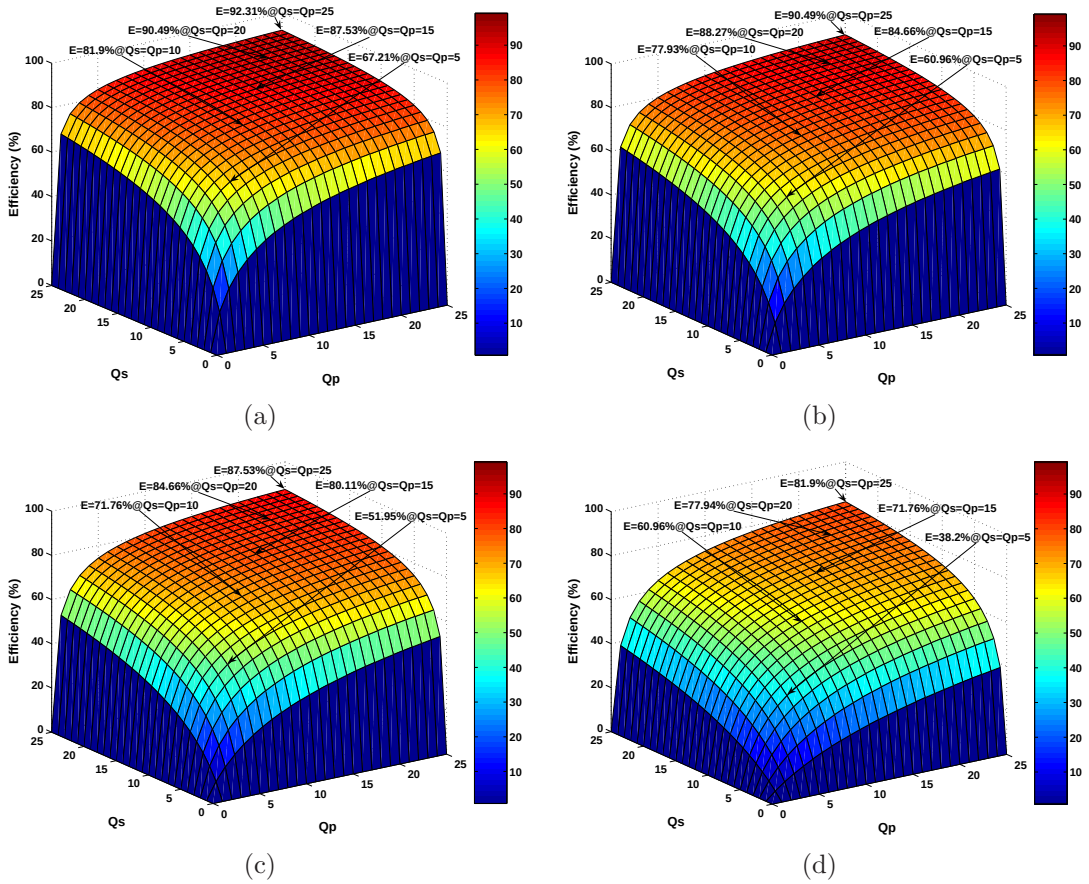


Figure 4.38: Efficiency of the transformer-based matching network: (a) K=1; (b) K=0.8; (c) K=0.6; (d) K=0.4.

$$G_{p,max} = 10 \log \left[\frac{|S_{21}|}{|S_{12}|} \left(K - \sqrt{K^2 - 1} \right) \right] \tag{4.112}$$

where

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{4.113}$$

and

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{4.114}$$

The loss of the transformer in the case of zero source admittance (idealised output of the transistor) can be expressed as:

$$Loss = -10 \log \frac{|S_{21}|^2}{1 - |S_{11}|^2} \tag{4.115}$$

The value in (4.115) equals to (4.112) when the output is loaded by the impedance for simultaneous conjugate match.

The values of the input(Γ_{Ms}) and output(Γ_{Ml}) reflection coefficients required for simultaneous conjugate match are:

$$\Gamma_{Ms} = \frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \tag{4.116}$$

and

$$\Gamma_{Ml} = \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2} \tag{4.117}$$

where

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \tag{4.118}$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 \tag{4.119}$$

$$C_1 = S_{11} - \Delta S_{22}^* \tag{4.120}$$

$$C_2 = S_{22} - \Delta S_{11}^* \tag{4.121}$$

The minus sign must be used in (4.116) and (4.117) when calculating the simultaneous conjugate match for an unconditionally stable two-port network [Gonzalez 97].

Finally the required impedances or admittances for the simultaneously match condition can be extracted from (4.116) and (4.117) as:

$$Z_{Ms} = Z_0 \frac{1 + \Gamma_{Ms}}{1 - \Gamma_{Ms}} \tag{4.122}$$

and

$$Z_{Ml} = Z_0 \frac{1 + \Gamma_{Ml}}{1 - \Gamma_{Ml}} \tag{4.123}$$

or

$$Y_{Ms} = \frac{1}{Z_{Ms}} \tag{4.124}$$

and

$$Y_{Ml} = \frac{1}{Z_{Ml}} \tag{4.125}$$

4.4 Final Design

The circuit diagram of the final design is shown in Fig. 4.39. It is a one stage push-pull CMOS power amplifier. It consists of two single transistors which are working in a differential mode that creates a virtual ground for the odd harmonics between the sources and relax requirements for the ground connection.

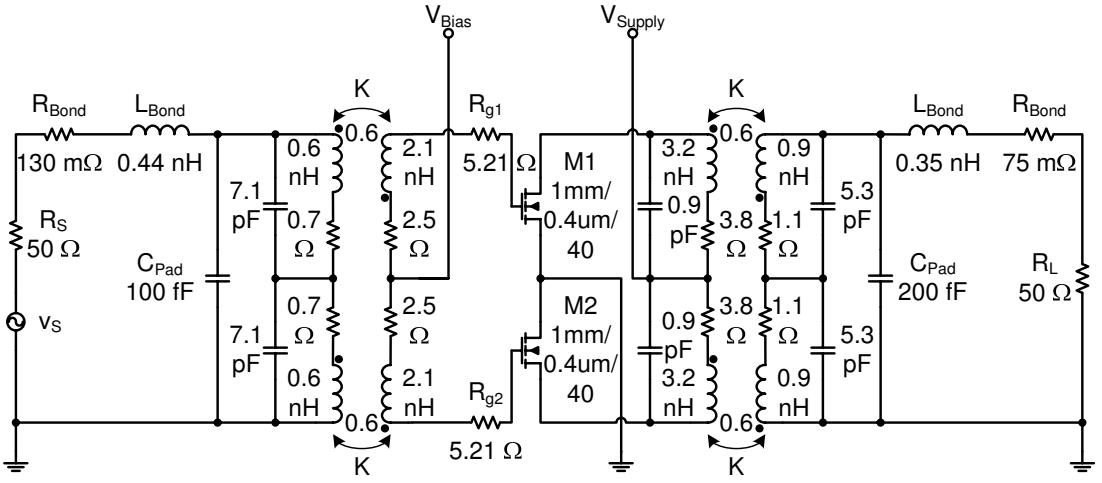


Figure 4.39: Circuit diagram of the one stage push-pull CMOS power amplifier.

The 50 Ω load resistance presents the prevalent characteristic impedance in the RF design. Then the output pad is bonded by two bond wires which series inductance of 0.35 nH and resistance of 75 mΩ are calculated in the previous part (see Fig. 4.35). The pad is modelled by the capacitor with a capacitance of 200 fF to the ground. The output transformer with capacitors perform the transformation of the single-ended impedance to the differential of $2(56.6 + j40.1)$ Ω (see drain load diff. in Fig. 4.40) that is estimated during the load-pull simulation (see Table 4.1). The input matching network (the input transformer and capacitors) transfers differential input impedance of the transistors of $2(6.2 + j30)$ Ω (see Table 4.1) into the single ended impedance. The input pad is two times smaller in comparison with the output one and it is modelled by the capacitor of 100 fF and bonded by the one bond wire with series inductance of 0.44 nH and series resistance of 130 mΩ (see Fig. 4.35). The component values of the input matching network is calculated in such way that input impedance of the power amplifier equals to 50 Ω (see input impedance in Fig. 4.40).

The transfer characteristic of the final power amplifier is shown in Fig 4.41. The power amplifier has the maximum power added efficiency of 39.2 % at the input power of 8 dBm with the output power of 14.2 dBm and drain efficiency of 51.6 %. The output power of the final power amplifier is about 1.1 dB higher as it is expected from the prototype design 11.4 dBm + 3 dB - 1.444 dB (where 11.4 dBm is the output power of the single ended prototype, 3 dB is an increase due to power

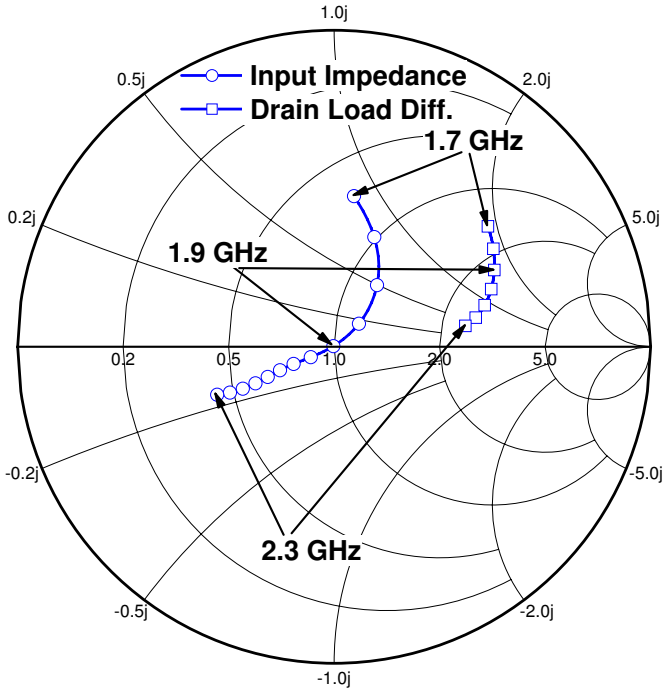


Figure 4.40: Frequency response of the input impedance and differential load of the drains of the one stage CMOS push-pull power amplifier. Z Smith chart is normalized to 50 Ω impedance.

combining of two amplifiers, - 1.444 dB is the loss of the output matching network). The output power increase is due to the fact that final transformer-based CMOS power amplifier operates similar to inverse Class-F amplifier [Wei 00] instead of Class-B operation of the designed CMOS prototype amplifier (compare Fig. 4.42 and Fig. 4.11).

Finally large-signal frequency response at input power of 8 dBm is shown in Fig. 4.43. The input power of 8 dBm is chosen in accordance with power transfer characteristic presented in Fig. 4.41 as the power added efficiency reaches its maximum at this input power. The frequency response shows that the maximums of the output power, drain efficiency and power added efficiency are very close to the chosen operating frequency of 1.9 GHz.

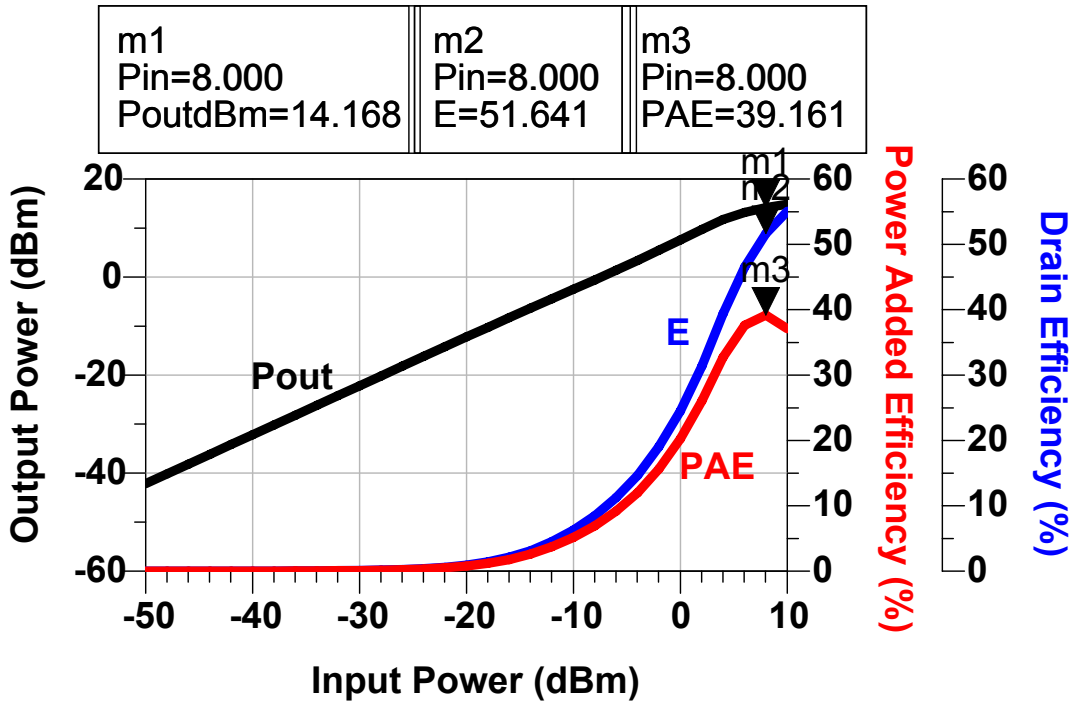


Figure 4.41: Transfer characteristics of the one stage push-pull CMOS power amplifier at the operating frequency of 1.9 GHz, showing output power (14.2 dBm) and drain efficiency (51.6 %) at the highest power added efficiency (39.2 %).

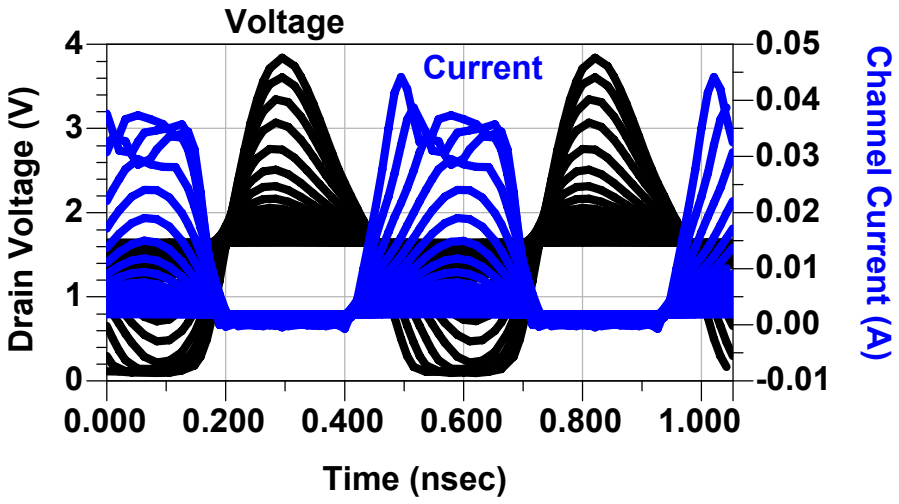


Figure 4.42: Drain voltage and channel current waveforms of the one shoulder, showing inverse Class-F operation of the push-pull transformer-based CMOS power amplifier.

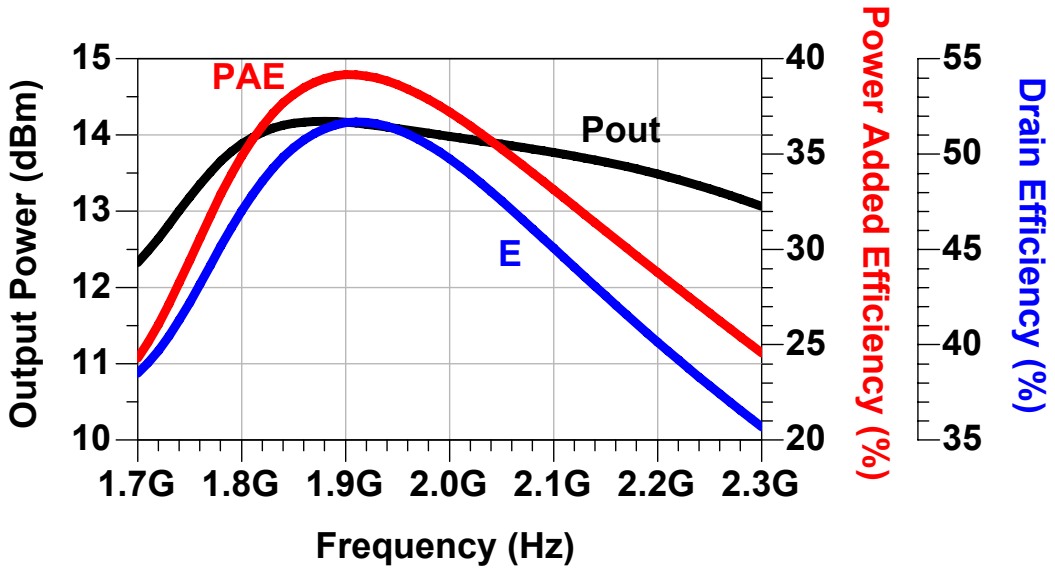


Figure 4.43: Frequency response of the one stage push-pull CMOS power amplifier at the input power of 8 dBm.

Chapter 5

Experimental Results

The aim of this work is the building of fully monolithically-integrated power amplifiers. The transformer-based push-pull architecture is used as the basic circuit for our investigation. The main advantage of the push-pull architecture is the relaxed requirements for the ground connections, but for the single ended input and output ports additional input and output baluns are required. At first the monolithically integrated power amplifiers with an external matching network are investigated. Fig. 5.1 gives an example of the two-stage transformer-based CMOS power amplifier with an external matching network [Vasylyev 04].

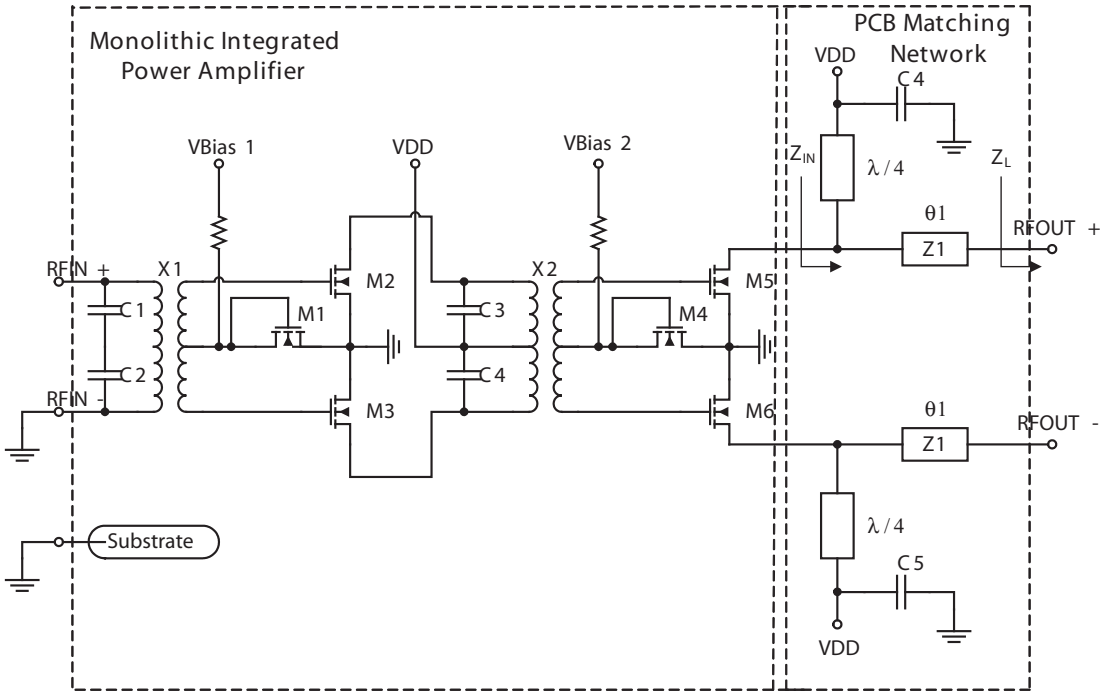


Figure 5.1: Circuit diagram of the power amplifier.

This power amplifier was mounted on the Rogers RO4003 microwave substrate

with a $\lambda/4$ matching network (see Fig. 5.2). The matching network requires an area of 25 mm x 50 mm.

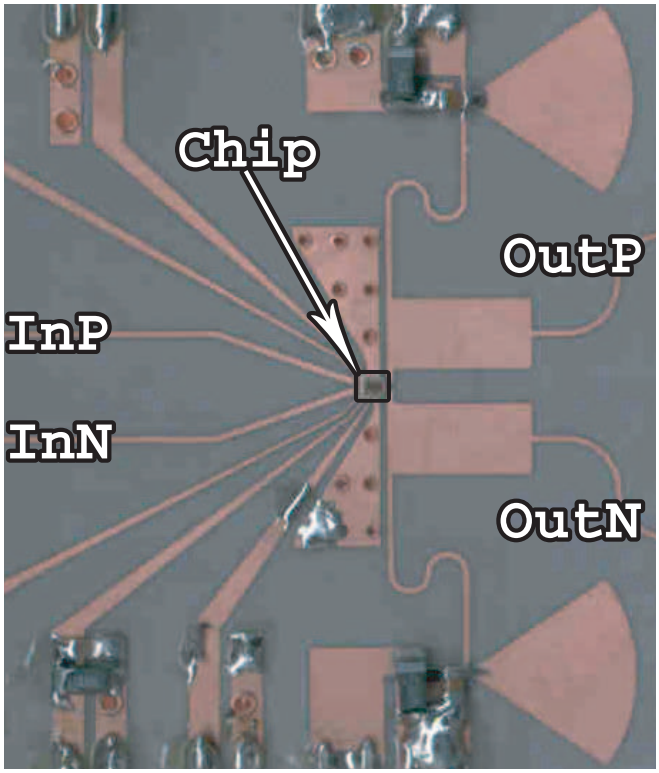


Figure 5.2: Photograph of the power amplifier board (size 50 mm x 50 mm).

As alternative solutions to the external matching network, following on chip matching network topologies are investigated: the LC-based network, transformer-based matching network and power combining transformer.

The LC-based network (see Fig. 5.3(a)) combines the functions of matching and phase inversion required for the proper push-pull operation. The components form complementary low-pass (C1, L1, L3) and high-pass (C2, L2, C3) circuits on respective push-pull shoulders with the same impedance transformation ratio. Additional a dc blocking capacitor C4 is added in front.

The transformer-based matching network (see Fig. 5.3(b)) consists of the transformer X1 with a center tap on the primary winding and capacitors C1, C2, and C3. The capacitors together with the winding inductances of the transformer form a parallel resonant tank.

If one transformer-based power amplifier is not able to deliver the required output power or bandwidth, the power combining transformer structure can be used [Vasylyev 05,b]. The power combining transformer shown in Fig. 5.3(c)) consists of four transformer-based networks. The secondary windings of transformers

X1, X2 and transformers X3, X4 are connected in series and then they are connected in parallel. Such connection of transformers in ideal case delivers the same impedance to each power amplifier as a single transformer.

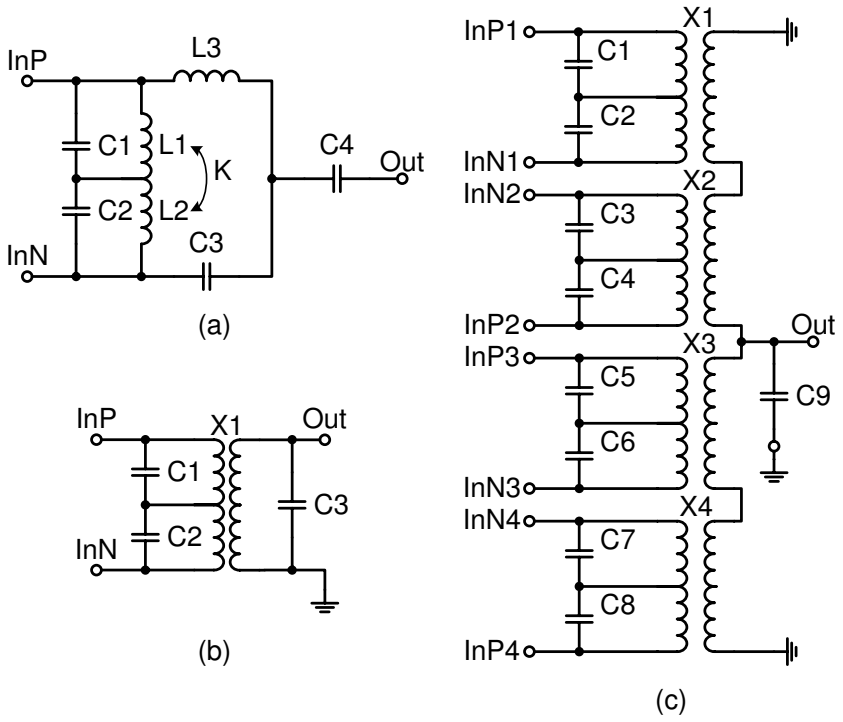


Figure 5.3: Output matching networks. Circuit diagrams: (a) LC-based matching network; (b) Transformer-based matching network; (c) Power combining transformer.

The 2 GHz realisations of the previously discussed matching networks are shown in Fig. 5.4. The inductors L1 and L2 of the LC-based matching networks (see Fig. 5.4(a)) are combined in to the one center-tapped inductor. The capacitor C4 is placed above the capacitor C3 to eliminate an additional parasitic capacitance to the lossy substrate at the output node of the matching network. This matching network occupies the area of 460 μm x 410 μm. The transformer-based matching network (see Fig. 5.4(b)) occupies the area of 330 μm x 380 μm. The power combined transformer structure shown in Fig. 5.4(c) has a four times larger area and equals to 1320 μm x 380 μm.

The amplifiers made during this work cover four frequency bands (2 GHz, 5 GHz, 17 GHz and 26 GHz) and use two technologies (a 0.13 μm CMOS and 28 GHz f_T SiGe-bipolar). Fig. 5.5 summarizes the performance of the power amplifiers. Also, the latest results of the fully monolithically integrated transformer-based power amplifiers are additionally highlighted by the red circle and described below in more detail.

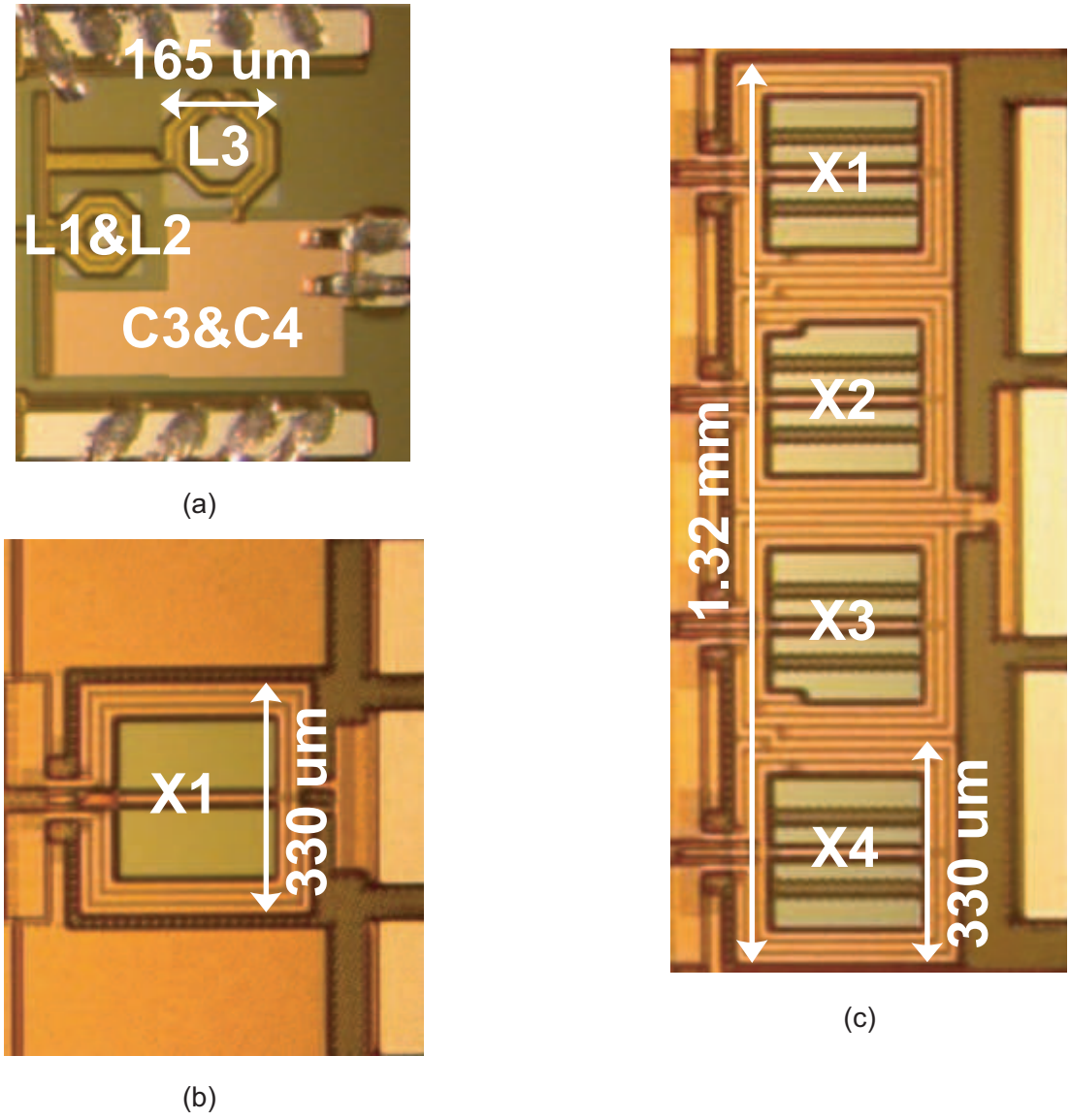
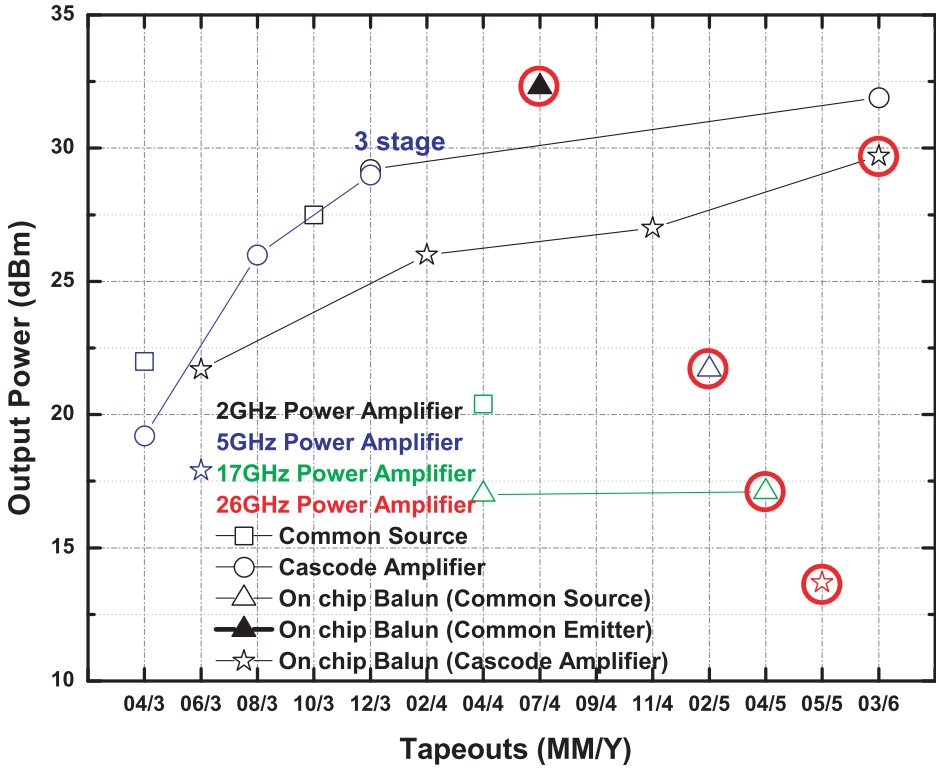
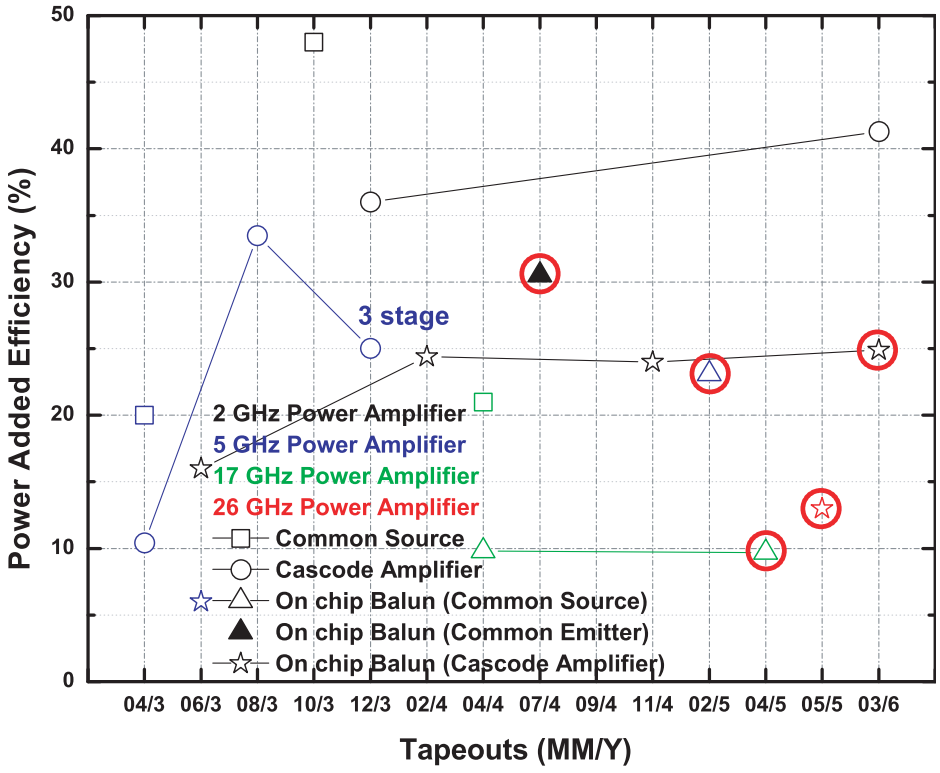


Figure 5.4: Chip photos of the 2 GHz output matching networks: (a) LC-based matching network; (b) Transformer-based matching network; (c) Power combining transformer.



(a)



(b)

Figure 5.5: Performance of the most interesting experimental results of the power amplifiers which are made during this work: (a) Output power; (b) Power added efficiency.

5.1 2 GHz CMOS Transformer-Based Power Amplifier

The circuit diagram of the fully monolithically-integrated CMOS DECT power amplifier is shown in Fig. 5.6. The thick gate oxide NMOS transistors in the cascode configuration are used in this design to satisfy the maximum power supply requirement of 3.5 V. A two stage configuration is used to amplify the input power of 5 dBm to the output power above 26.5 dBm (in accordance with DECT specification).

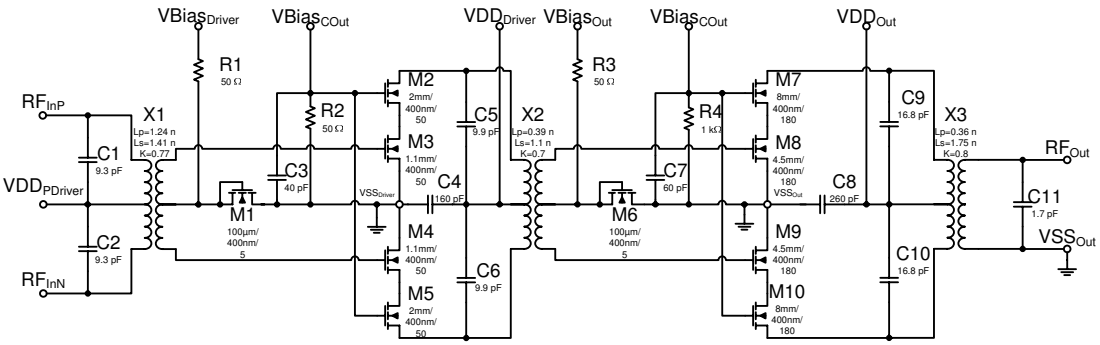
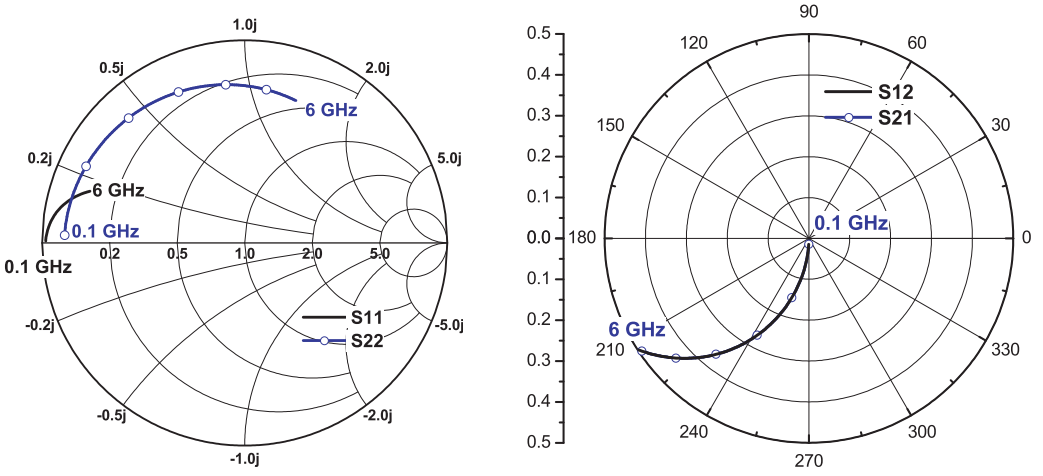


Figure 5.6: Simplified circuit diagram of the 2 GHz CMOS fully integrated power amplifier.

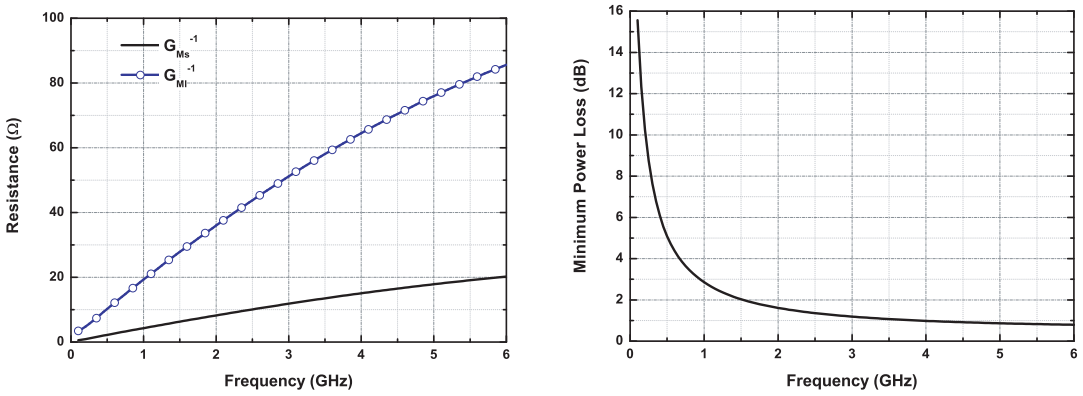
The output matching network is a crucial component of the power amplifier; and the output transformer has the highest influence on its performance. The simulated differential S-parameters of the output transformer are shown in Fig. 5.7.



(a) (b)

Figure 5.7: S-parameter simulation results for the output transformer: (a) S11, S22; (b) S12, S21.

The inverse of the real part of the required admittances for the simultaneously match condition are shown in Fig. 5.8(a). The minimum power loss of 1.68 dB at the frequency of 1.9 GHz under above condition can be achieved for the parallel source resistance of 7.8 Ω and parallel load resistance of 34.4 Ω (see Fig. 5.8(b)).



(a) (b)

Figure 5.8: Output transformer simulation results: (a) Parallel source and load resistances required for the simultaneous conjugate match condition; (b) Minimum power loss.

The simplified circuit diagram of the transformer-based matching network is shown in Fig. 5.9. The matching network consists of the transformer X3, tuning capacitor C11 and parasitic elements of bond wires Lb1, R1, Lb2 and R2. The value of the capacitor C11 is optimized to reduce the power loss of the matching network.

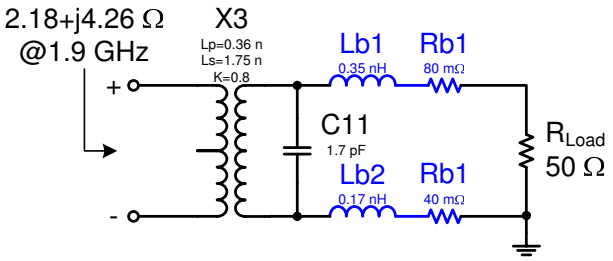
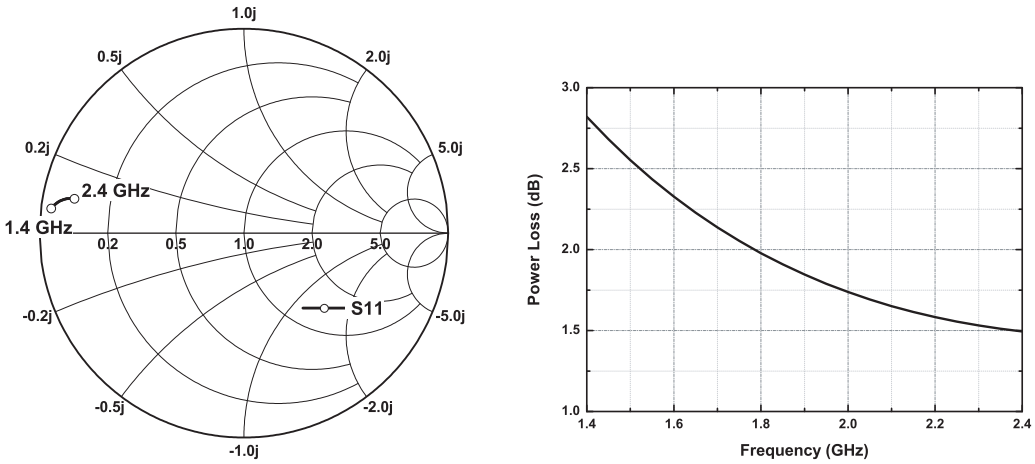


Figure 5.9: Transformer-based output matching network.

The input impedance and power loss of the output matching network are shown in Fig. 5.10. The output matching network has 1.85 dB of power loss and transforms the single ended 50 Ω load into the differential input impedance of 2.18+j4.26 Ω at 1.9 GHz. In the final circuit (see Fig. 5.6), the capacitors C9 and C10 as well as parasitic output capacitances of the transistors M7, M8, M9 and M10 compensate the imaginary part that gives the final impedance of 10.5 Ω.



(a) (b)

Figure 5.10: Simulation results of the output transformer-based matching network: (a) S11; (b) Power loss.

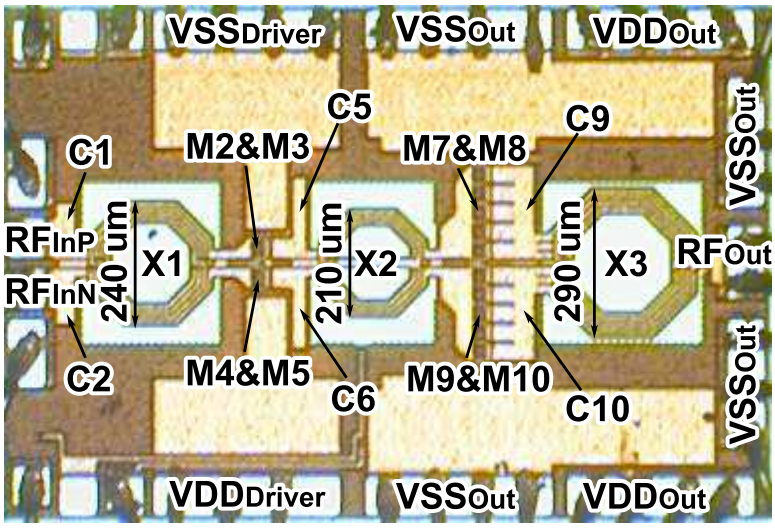


Figure 5.11: Die photograph of the fully integrated power amplifier (size 1.5 mm x 1 mm).

The chip photo of the fabricated power amplifier in a 0.13 μm CMOS process for RF applications is shown in Fig. 5.11. As can be seen all transformers have a symmetrical octagonal configuration to improve the quality factor.

The measured frequency responses of the power amplifier for 2 V, 2.5 V, 3 V and 3.5 V supplies with the input power of 5 dBm are shown in Fig. 5.12. The power transfer characteristics for the same voltage conditions at 1.9 GHz are shown in Fig. 5.13. The output power of 28.2 dBm with the power added efficiency of 22.4 % is achieved at the frequency of 1.9 GHz and the supply voltage of 3.5 V. The small signal gain is 29 dB at 1.9 GHz

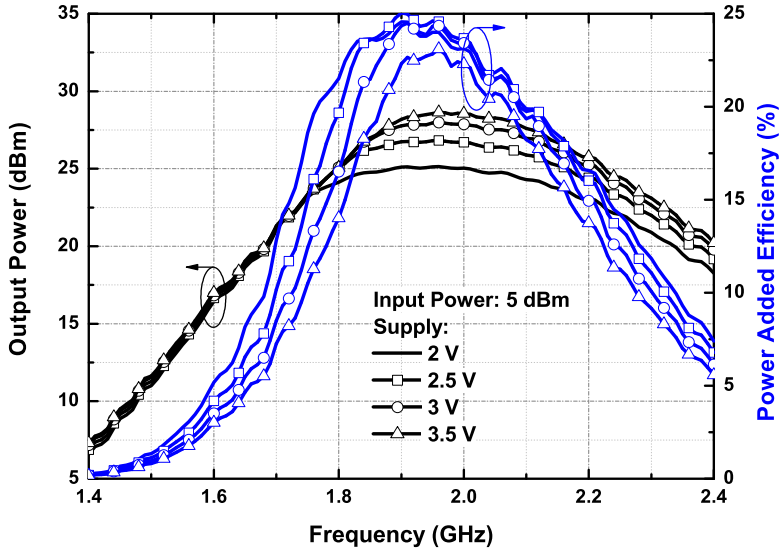


Figure 5.12: Measured frequency response of the fully integrated power amplifier.

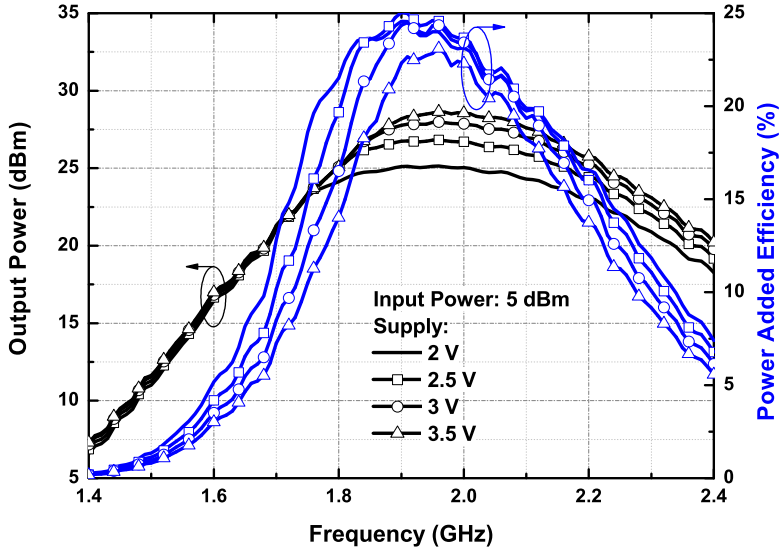


Figure 5.13: Measured power transfer characteristics of the fully integrated power amplifier.

5.2 5 GHz CMOS Transformer-Based Power Amplifier

The circuit diagram of the CMOS fully monolithically-integrated power amplifier for the WLAN 802.11a is shown in Fig. 5.14. The power amplifier is implemented in a 0.13 μm RF CMOS technology.

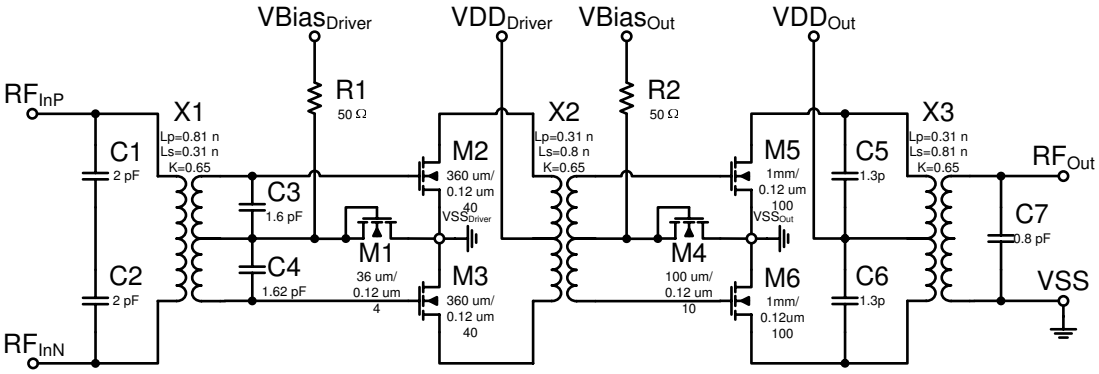
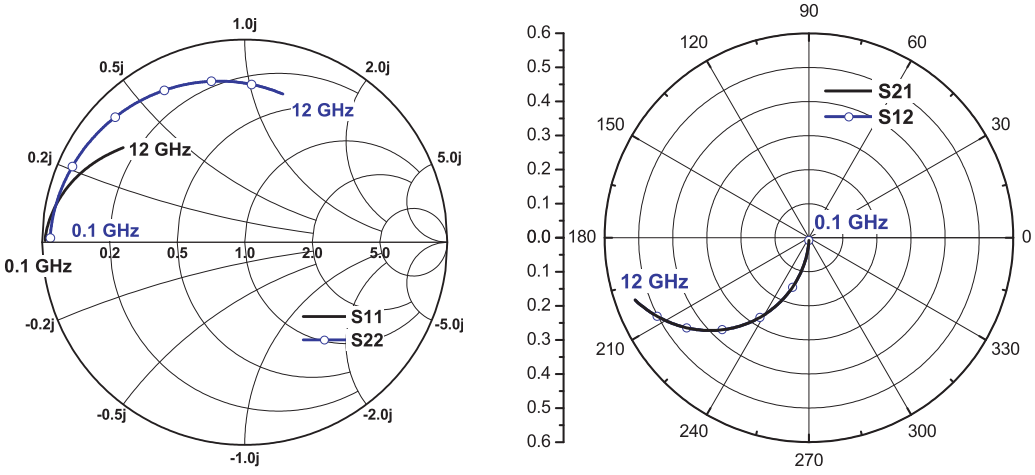


Figure 5.14: Simplified circuit diagram of the fully integrated power amplifier.

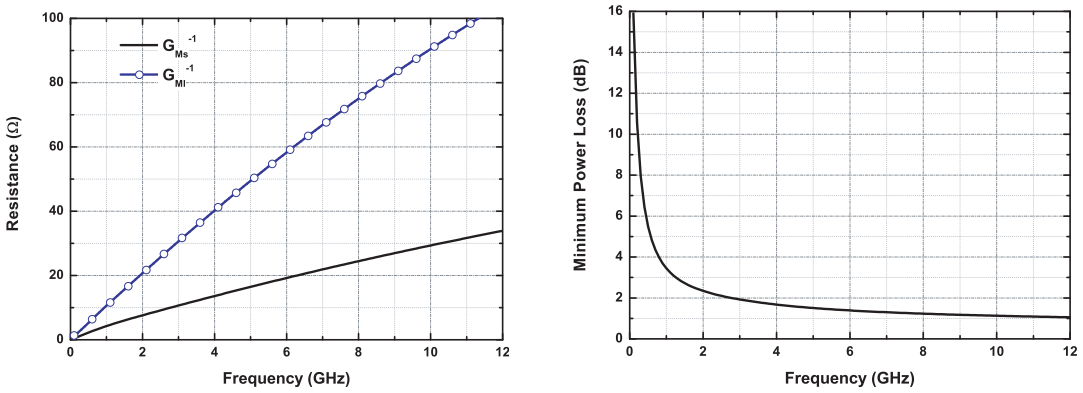
The S-parameter simulation results of the output transformer in the frequency range from 0.1 GHz to 12 GHz are shown in Fig. 5.15.



(a) (b)

Figure 5.15: Differential S-parameters of the output transformer: (a) S11, S22; (b) S12, S21.

The minimum power loss under the simultaneous match condition at 5.5 GHz is 1.44 dB (see Fig.5.16(b)). The inverse of the real part of the source admittance equals to 17.9 Ω and the inverse of of the real part of the load admittance equals to 53.9 Ω (see Fig.5.16(a)).



(a) (b)

Figure 5.16: Simulation results of the output transformer: (a) Parallel source and load resistances required for the simultaneous conjugate match condition; (b) Minimum power loss.

The output matching network is shown in Fig. 5.17 and consists of the output transformer X3, tuning capacitor C7, pads parasitic elements Rp1, Cp1, Rp2, Cp2 and bond wires parasitic elements Lb1, Rb1, Lb2 and Rb2.

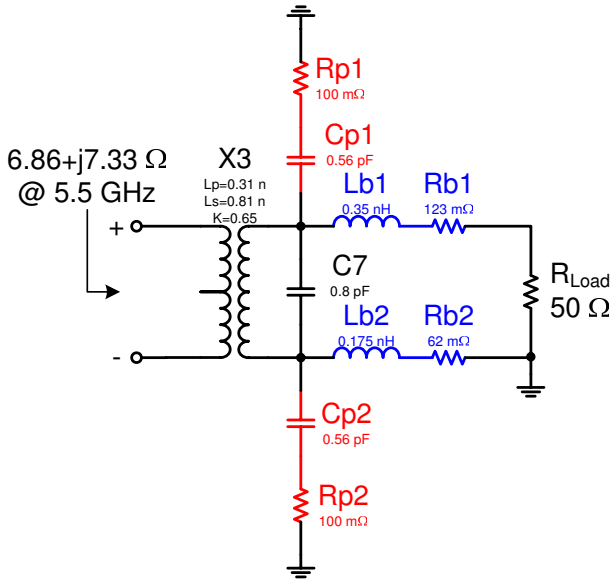
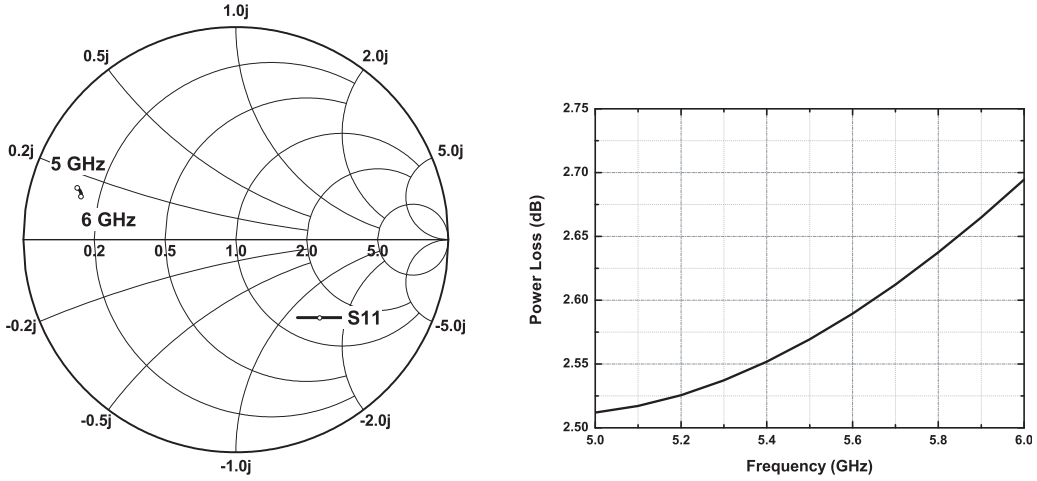


Figure 5.17: Transformer-based output matching network.

The input impedance of the output matching network equals 6.86+j7.33 Ω at 5.5 GHz (see Fig. 5.18(a)). The additional matching capacitors C5 and C6 in parallel with the parasitic capacitors of the transistors M5 and M6 are included in the final circuit (see Fig. 5.14) to compensate the imaginary part of the input impedance of the output matching network. That gives the final differential

impedance of 14.7 Ω. The output matching networks has the power loss of 2.57 dB (see Fig. 5.18(b)). The later simulation has shown that the pad parasitics (C1 and R1) at the RF output cause about 1 dB of the power loss. The pad size reduction or a shielding of the pad from the lossy substrate can help to reduce the power loss. Unfortunately it was not implemented for this design.



(a) (b)

Figure 5.18: Simulation results of the output matching network: (a) S11; (b) Power loss.

Fig. 5.19 shows the chip photograph of the manufactured fully-integrated power amplifier. The die size is 1 mm x 1 mm.

The measured frequency response of the power amplifier at the input power of 10 dBm is shown in Fig. 5.20. The output stage is supplied by 1.5 V and the driver stage by 0.75 V. The power amplifier delivers the saturated output power of 21.7 dBm with the power added efficiency of 23.1 % at the frequency of 5.5 GHz (see Fig. 5.21).

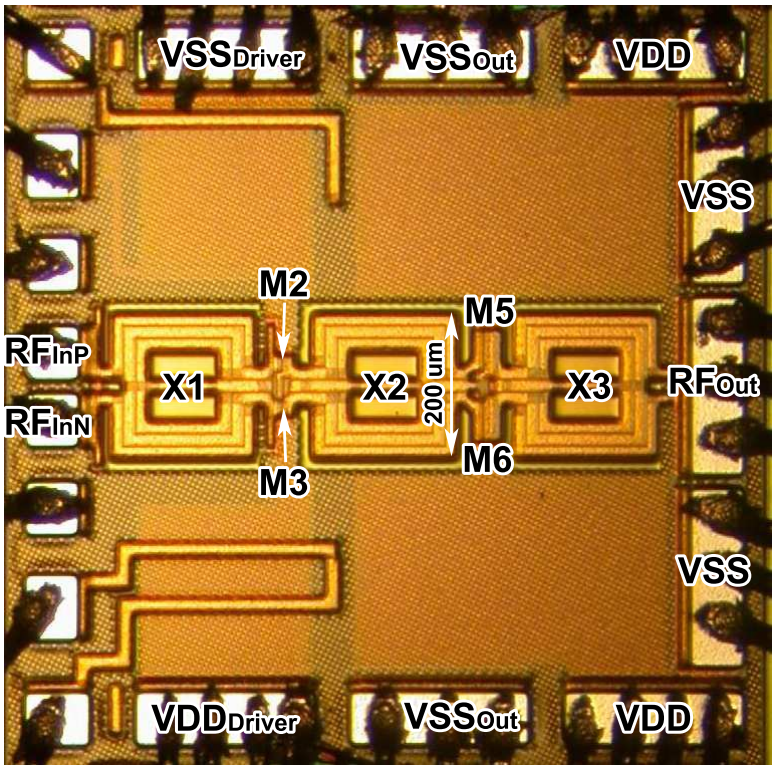


Figure 5.19: Die photograph of the fully integrated power amplifier (size 1 mm x 1 mm).

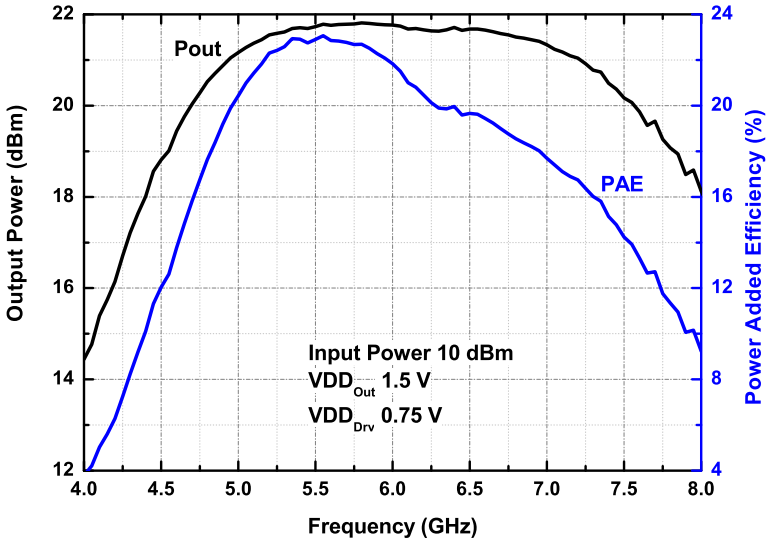


Figure 5.20: Measured frequency response of the fully integrated power amplifier.

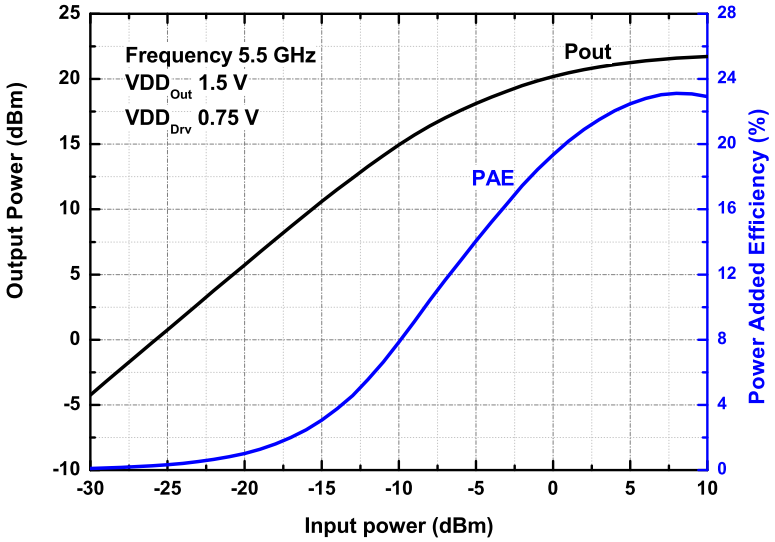


Figure 5.21: Measured power transfer characteristic of the fully integrated power amplifier.

Additionally, the power amplifier was tested with a OFDM input signal (WLAN 802.11a, 52 subcarriers, 16QAM, 36 Mbps). The EVM versus average output power is shown in Fig. 5.22. The transmit EVM for the data rate of 36 Mbps should not exceed 11.2 % in accordance with the WLAN 802.11a specification. The input signal with the average input power of 7 dBm that corresponds to the average output power of 16.3 dBm at EVM of 9.2 % is used for the next power amplifier tests. The complementary cumulative distribution function of the

power amplifier is shown in Fig. 5.23. The corresponding constellation diagram and output spectrum are shown in Fig. 5.24 and Fig. 5.25.

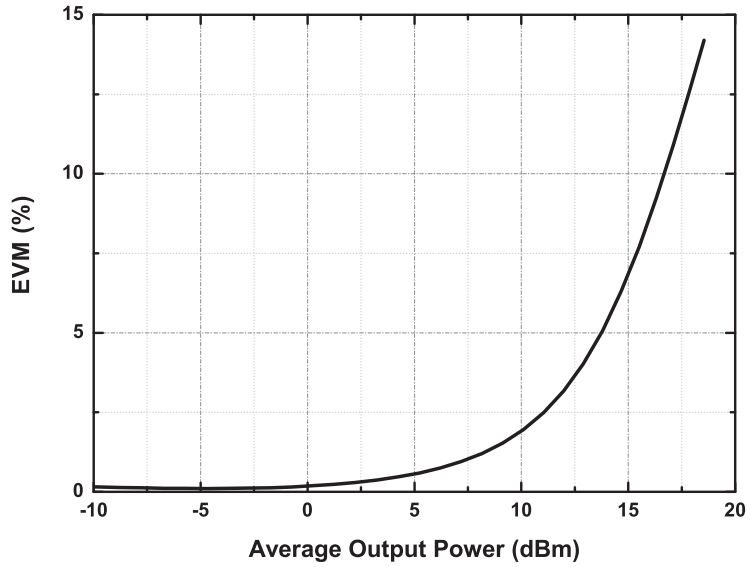


Figure 5.22: Experimental results of the power amplifier with OFDM input signal (WLAN 802.11a, 52 subcarriers, 16QAM, 36 Mbps), showing the error vector magnitude.

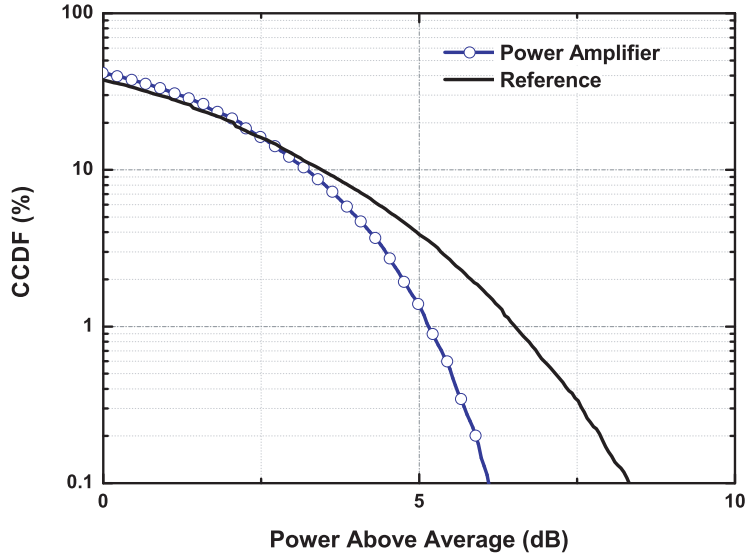


Figure 5.23: Complementary cumulative distribution function of the power amplifier at the EVM of 9.2 %.

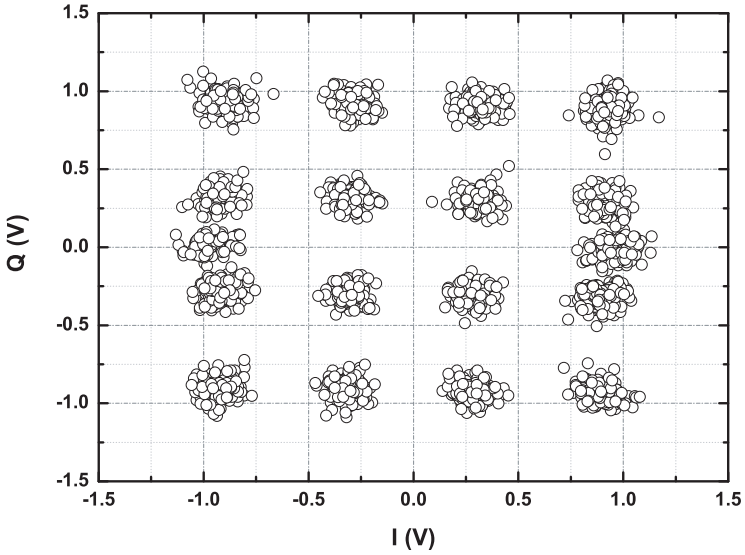


Figure 5.24: Constellation diagram of the power amplifier at the EVM of 9.2 %.

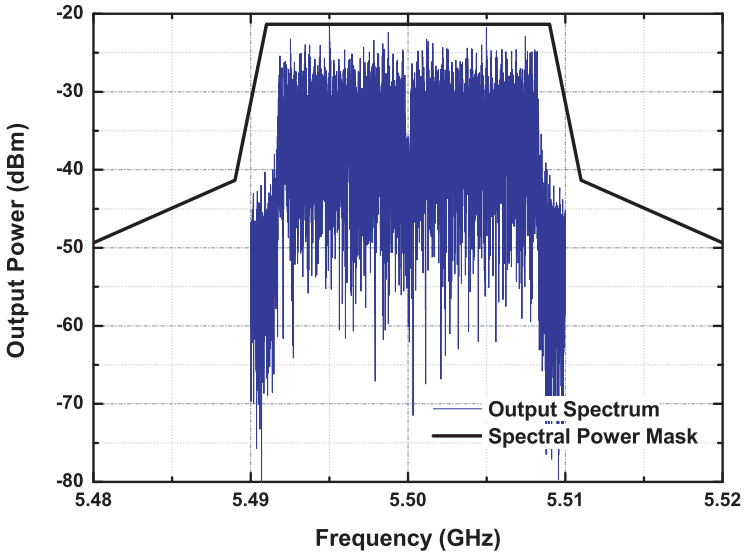


Figure 5.25: Output spectrum of the power amplifier with OFDM input signal (WLAN 802.11a, 52 subcarriers, 16QAM, 36 Mbps) at the EVM of 9.2 %.

5.3 17 GHz CMOS Transformer-Based Power Amplifier

The 17 GHz CMOS transformer-based power amplifier is designed in a standard 0.13 μm digital CMOS technology for the operation at the 1.5 V supply voltage [Vasylyev 06]. The simplified circuit diagram of it is shown in Fig. 5.26.

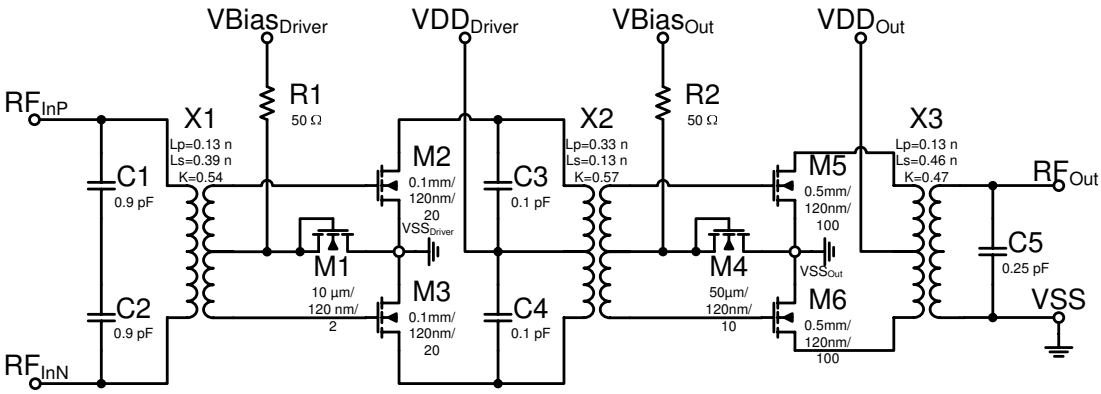
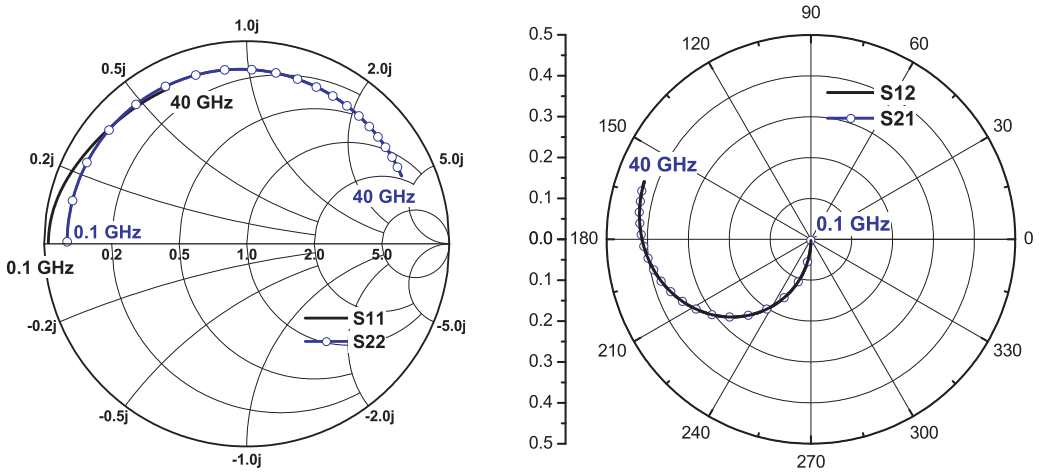


Figure 5.26: Simplified circuit diagram of the fully integrated power amplifier.

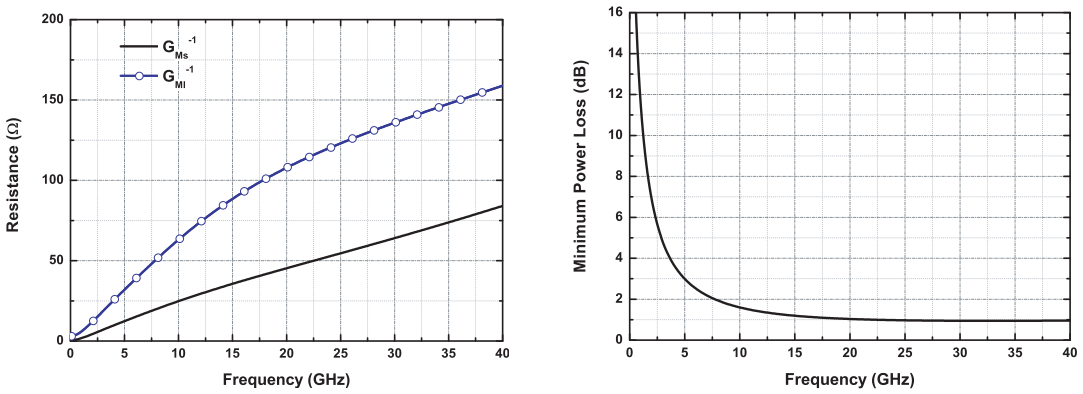
The power amplifier core consists of two push-pull amplification stages. The input, interstage and output matching networks are realised with parallel resonant circuits based on the inductance of the monolithically integrated transformers X1, X2 and X3 correspondingly. The bias networks are simple current mirrors providing a high flexibility in the investigation of the circuit.



(a) (b)

Figure 5.27: Differential S-parameter of the output transformer: (a) S11, S22; (b) S12, S21.

The differential S-parameters of the output transformer are shown in Fig. 5.27. The minimum power loss under the simultaneous match condition is estimated and is shown in Fig. 5.28(b). The inverse of the real part of the required admittances for the simultaneous match condition for the source is 40 Ω and for the load is 97.6 Ω.



(a) (b)

Figure 5.28: Output transformer: (a) Parallel source and load resistances required for the simultaneous conjugate match condition; (b) Minimum power loss.

The circuit diagram of the transformer-based output matching network is shown in Fig. 5.29. The bond wires and output pads transform the 50 Ω load impedance in 67+j45 Ω at 17.2 GHz; then it is further transformed by the matching capacitor C5 and transformer X3 to the impedance required for the best performance of the power amplifier.

The frequency response of the input impedance as well as the power loss of the output matching network are shown in Fig. 5.30. The final output matching network has the power loss of 4.1 dB at 17.2 GHz and delivers the differential impedance of 5.9+j11.3 Ω to the output of the power transistors M5 and M6.

Fig. 5.31 shows the die photograph of the designed power amplifier which has a size of 0.9 mm x 1 mm. All capacitors are parallel plate capacitors and have one plate on the AC ground (except C1 and C2 their bottom plates are just connected together) that avoids a lossy parasitic capacitance in to the substrate and improves their RF performance. The transformers have an octagonal symmetric layout that has a higher quality factor in comparison with a square symmetric one. Two uppermost copper layers were used as main wires for the transformers implementation.

The frequency response of the power amplifier is shown in Fig. 5.32. It delivers the output power of 16.8 dBm at 17.2 GHz that corresponds to the maximum PAE of 9.7 % with 7 dBm input power. The power transfer characteristic at 17.2 GHz is shown in Fig. 5.33. The small signal gain is 14.5 dB. The amplifier has an output 1 dB compression point of 15 dBm with the corresponding PAE of 7.8 %.

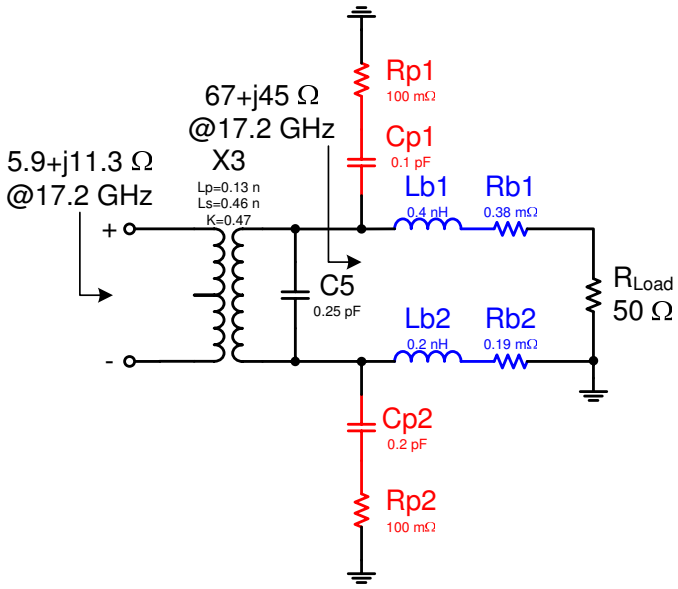
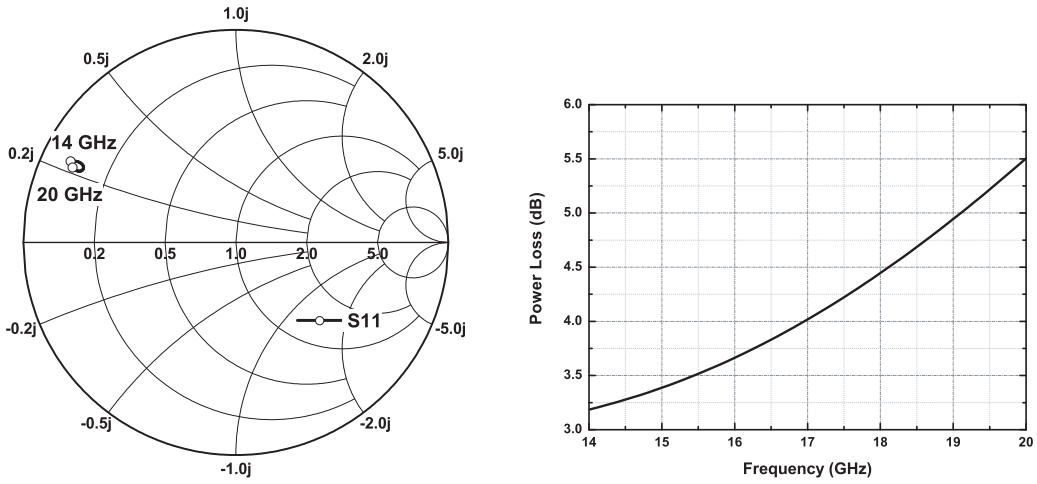


Figure 5.29: Circuit diagram of the output matching network.



(a) (b)

Figure 5.30: Simulation results of the output matching network: (a) S11; (b) Power loss.

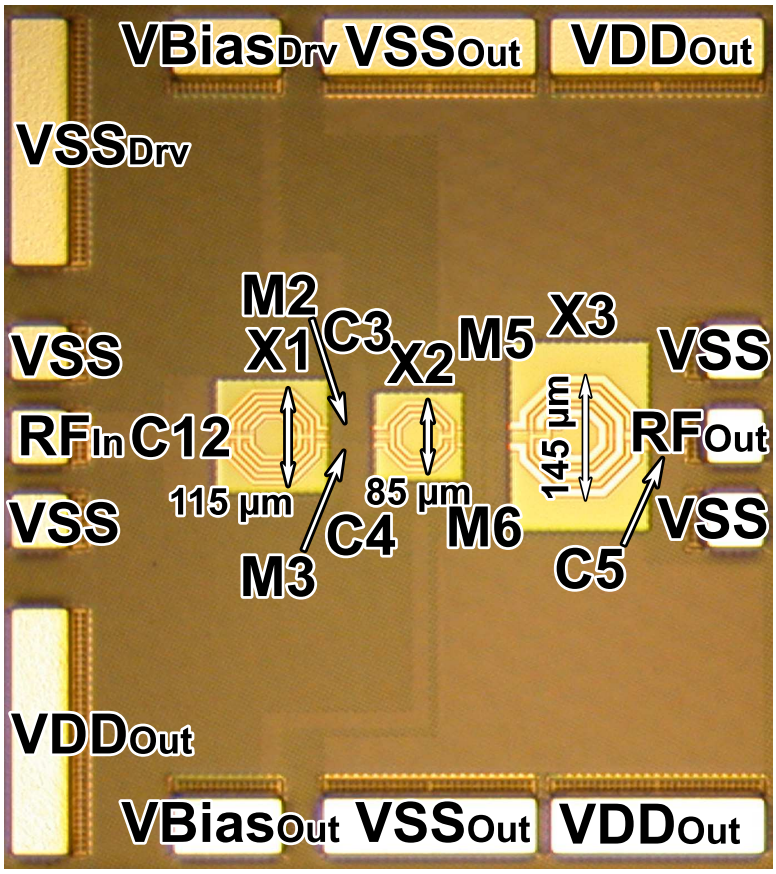


Figure 5.31: Die photograph of the fully integrated power amplifier (size 0.9 mm x 1 mm).

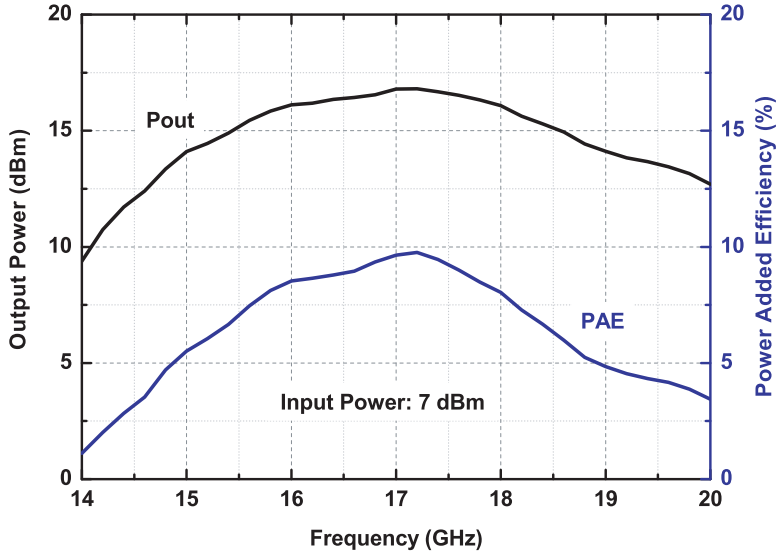


Figure 5.32: Measured frequency response of the fully integrated power amplifier.

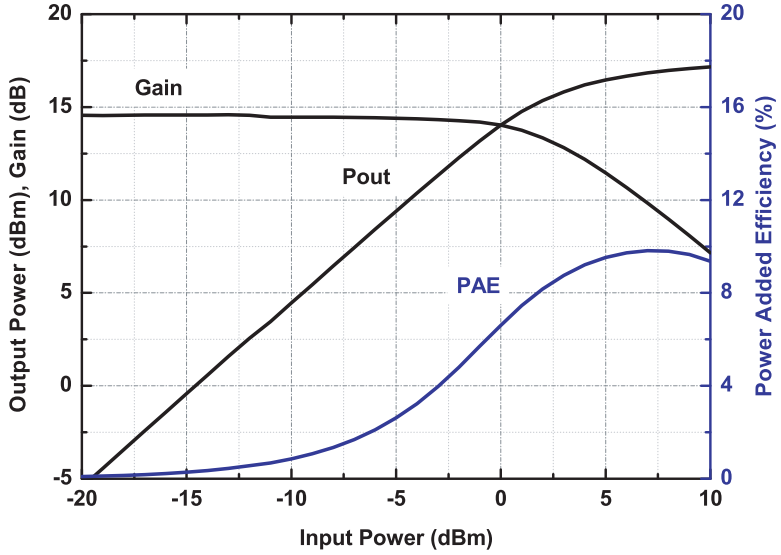


Figure 5.33: Measured power transfer characteristic of the fully integrated power amplifier.

5.4 26 GHz CMOS Transformer-Based Power Amplifier

The circuit diagram of the fully integrated 26 GHz CMOS power amplifier is shown in Fig. 5.34. It is a one-stage push-pull power amplifier which consists of a monolithic input and output transformers, two bias current mirrors, and amplifying transistors. The transformer X1 at the input transforms a single ended signal from a 50 Ω source to a differential signal which is driving the gates of the transistors. At the output the transformer X2 converts the differential signal on the drains (M4-M7) to a single ended signal which drives the 50 Ω load. In addition both transformers (X1, X2) perform an impedance matching and a dc decoupling. The current mirror (R1, M1) is used to provide a Class-AB operating point for the transistors (M5, M6) in common-source configuration. On the gates of the transistors M5, M6 exist the AC signal, the bias voltage is applied through the secondary center-tapped winding of the transformer X1. The current mirror (R2, M2, and M3) is used to provide an operating point for the cascode transistors (M4 and M7) in common-gate configuration. AC ground has to be on the gates of the transistors M4 and M7. The supply voltage for the output transistors is applied through the center tap of the transformer X2.

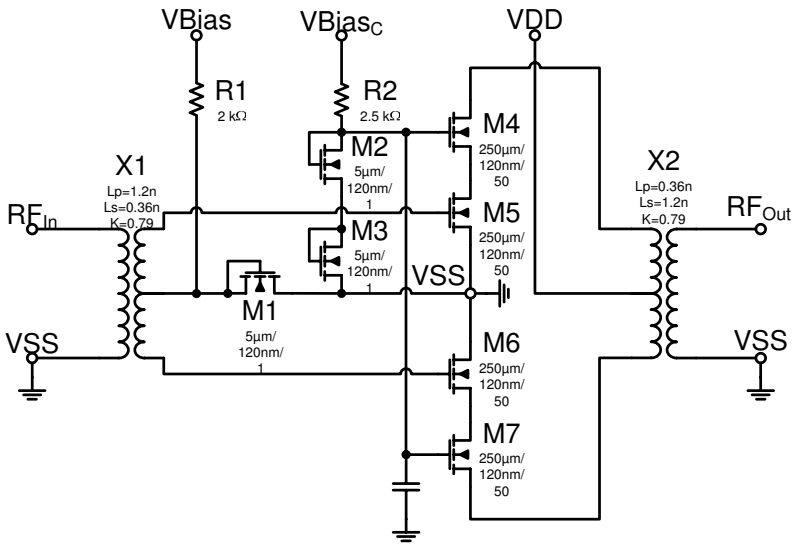
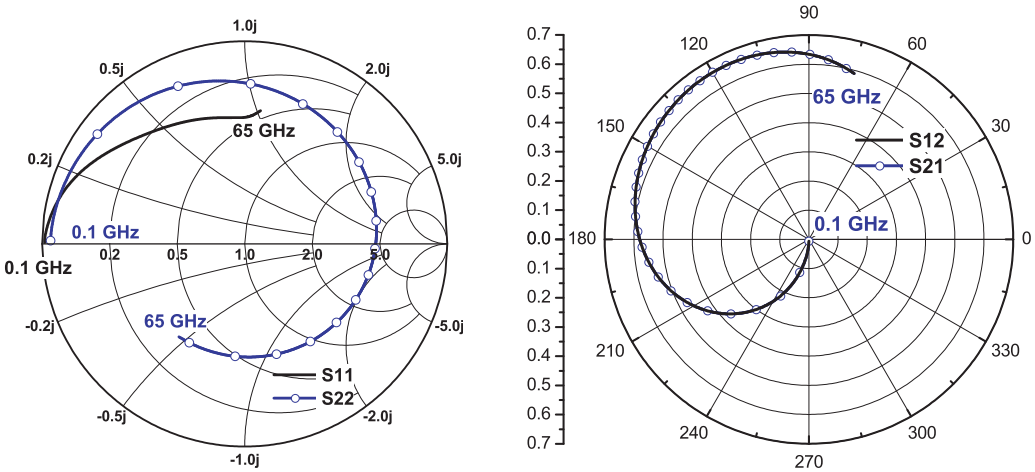


Figure 5.34: Simplified circuit diagram of the power amplifier.

The current mirrors transistors M1, M2, and M3 are one-finger transistors with a drawing width of 5 μm and a drawing length of 0.12 μm. The RF transistors M4, M5, M6, and M7 are fifty-finger transistors with a drawing width of 250 μm and a drawing length of 0.12 μm. All passive elements such as transformers, pads, and interconnections were modelled by S-parameters which were extracted from the layout by a 2.5D electromagnetic simulator. The lumped elements of

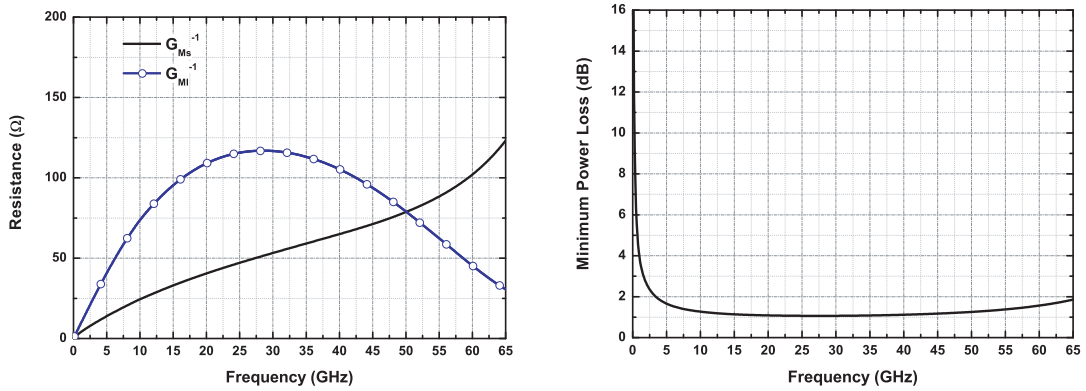
the transformers such as the primary winding inductance (Lp), the secondary winding inductance (Ls), and the coupling factor (K) were extracted from the S-parameters for the winding scheme of the transformers X1 and X2 which are identical and are shown in Fig. 5.34.

The simulated S-parameters of the transformers are shown in Fig. 5.35 where S11 corresponds to the primary winding of the transformer X2. The extracted parallel source and load impedances required for the simultaneously match condition are shown in Fig. 5.36(a). Fig. 5.36(b) shows the minimum power loss of the designed transformers which equals to 1.1 dB at the frequency of 25.7 GHz.



(a) (b)

Figure 5.35: Differential S-parameters of the transformers: (a) S11, S22; (b) S12, S21.



(a) (b)

Figure 5.36: Simulation results of the transformers: (a) Parallel source and load resistances required for the simultaneous conjugate match condition; (b) Minimum power loss.

The simplified circuit diagram of the output matching network is shown in Fig. 5.37.

The output matching network transforms a 50 Ω single ended load to the differential impedance of 11.6+j31.2 Ω at 25.7 GHz (see Fig. 5.38) which imaginary part is compensated by the parasitic capacitances of the output transistors. The power loss of the output matching network is 2.1 dB at the frequency of 25.7 GHz.

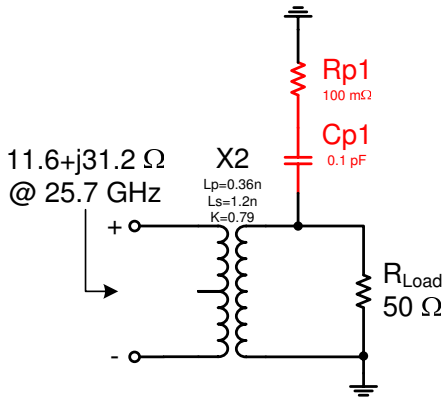
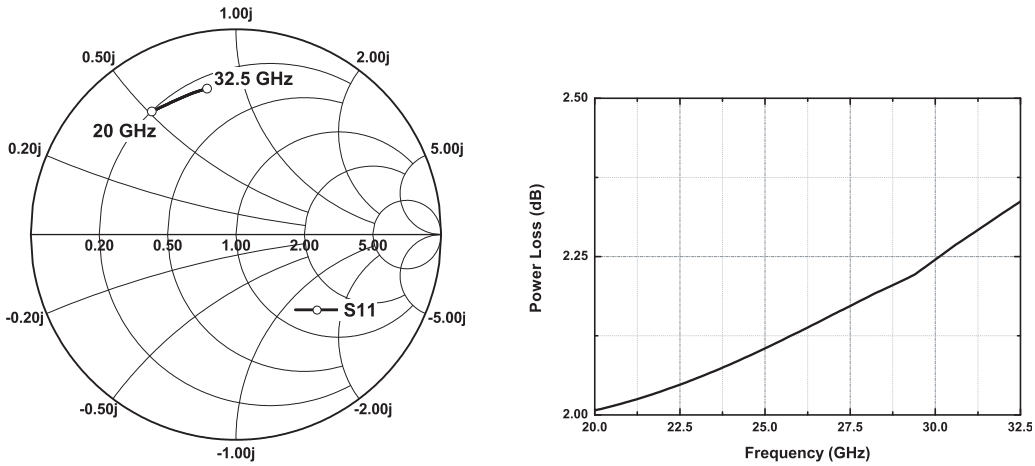


Figure 5.37: Simplified circuit diagram of the output matching network.



(a) (b)

Figure 5.38: The simulation results of the output matching network: (a) S11; (b) Power loss.

The power amplifier chip photo is shown in Fig. 5.39. The chip size is 1 mm x 1 mm. The input and output RF pads are configured for the G-S-G microwave probe with a pitch of 100 μm.

The measured and simulated frequency responses are shown in Fig. 5.40. The measured small-signal gain has a maximum at 25.7 GHz and equals to 8.4 dB. The power amplifier has a 3 dB bandwidth of 10.5 GHz that is between 20.5 GHz and 31 GHz. The measured and simulated power transfer characteristics at 25.7 GHz are shown in Fig. 5.41. At this frequency the power amplifier has a maximum

PAE of 13 % with the corresponding output power of 13 dBm at a supply voltage of 1.5 V. The measured and simulated results show a good agreement.

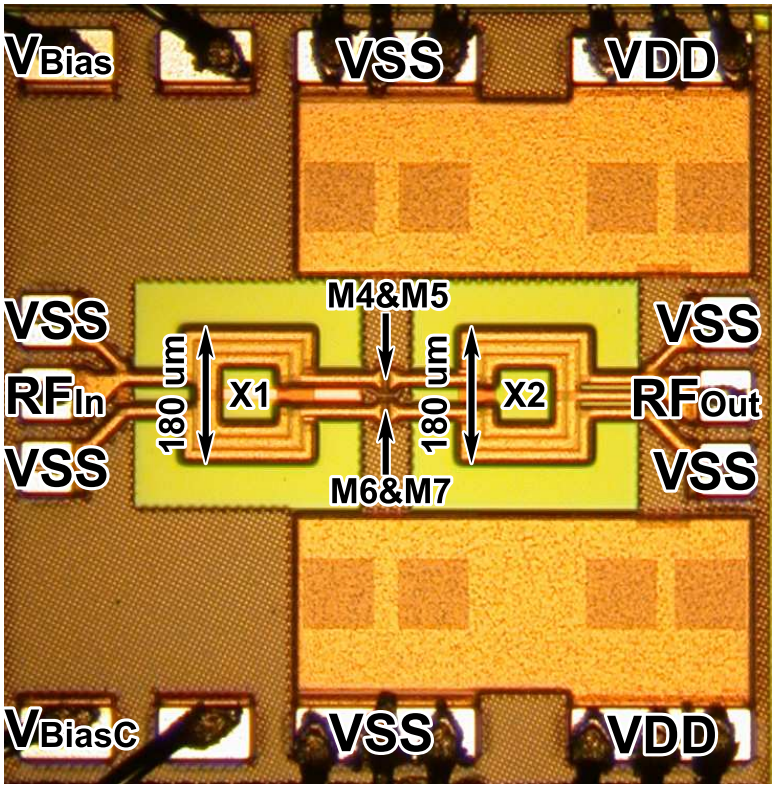


Figure 5.39: Die photograph of the power amplifier (size 1 mm x 1 mm).

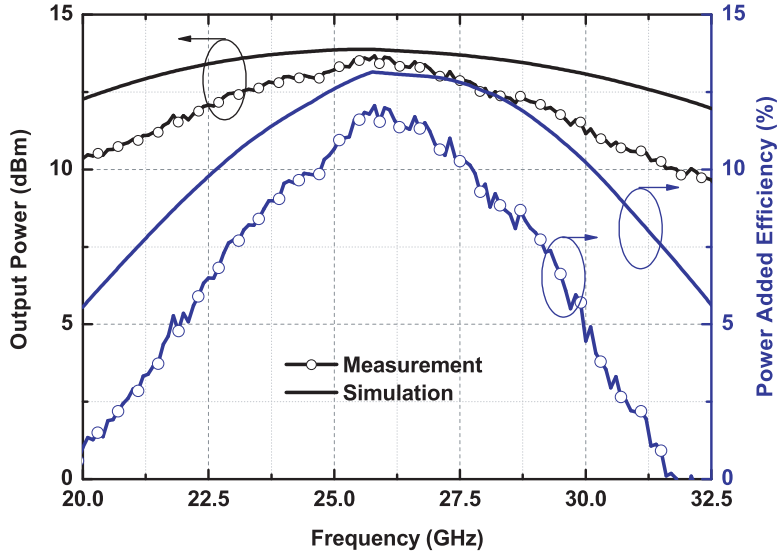


Figure 5.40: Frequency response of the power amplifier (measurement versus simulation).

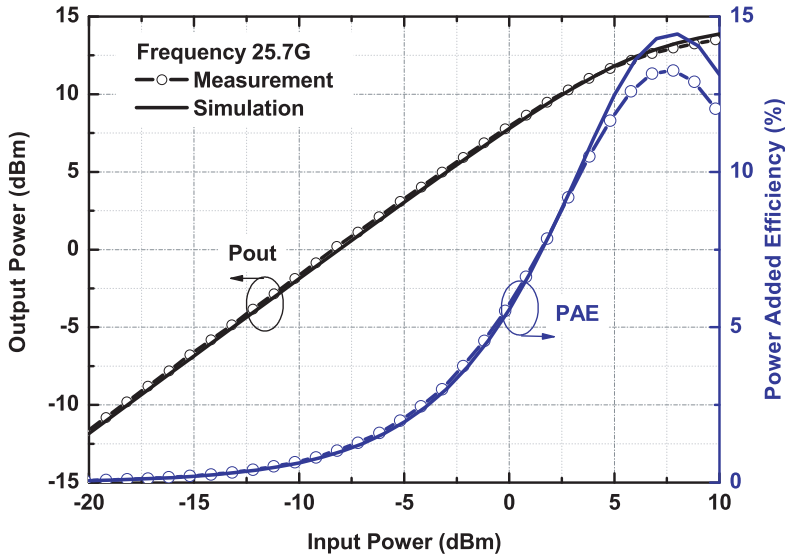


Figure 5.41: Transfer characteristics of the power amplifier (measurement versus simulation).

5.5 2 GHz Bipolar Power Amplifier Using the Power Combining Transformer

The circuit diagram of the fully monolithically-integrated 2 GHz bipolar power amplifier is shown in Fig. 5.42. It consists of four two-stage push-pull power amplifiers that are combined at the input and output by the power combining transformers. The single-ended 50 Ω input is converted by the four input transformers to the four balanced inputs of the driver stages. The secondary winding of this transformer is center-tapped for the bias voltage of the driver stage.

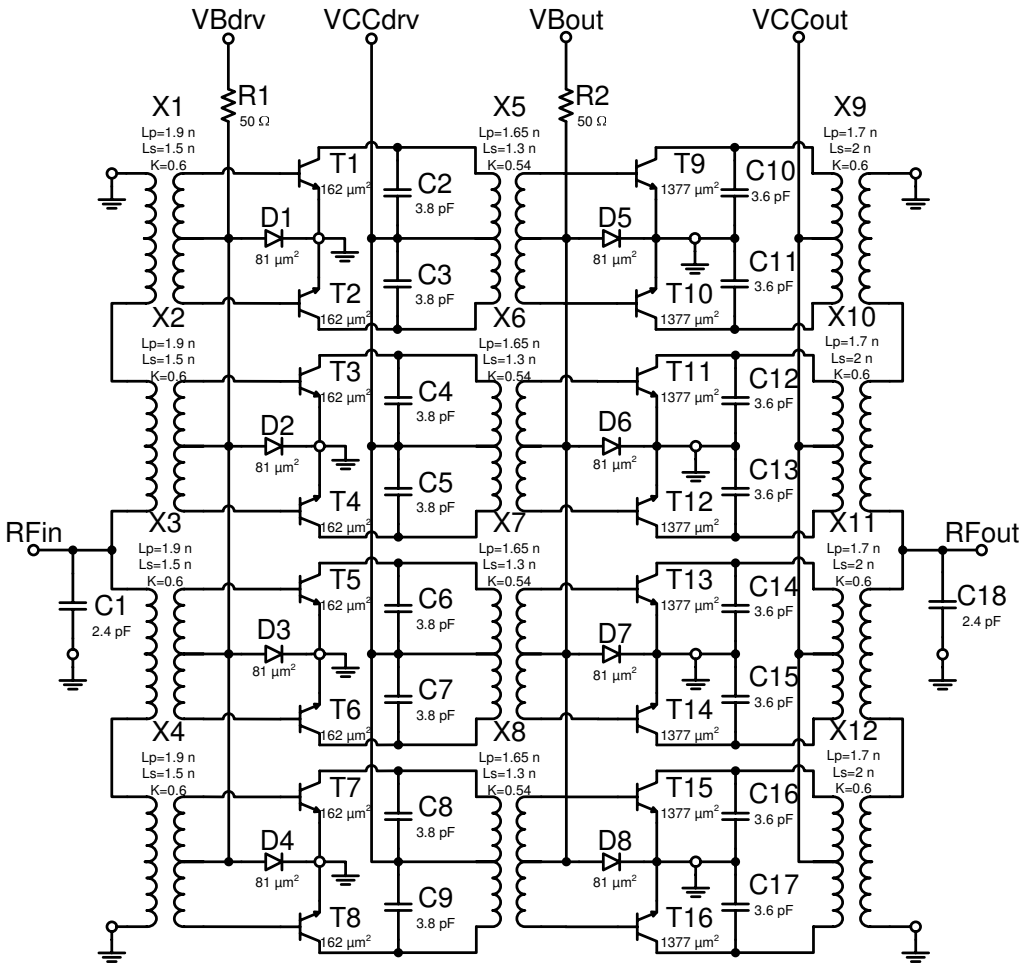


Figure 5.42: Circuit diagram of the power amplifier.

Each driving stage (four in total) is loaded by a pair of transformers with center tapping for driver supply voltage and bias for the final stage. In parallel to the primary winding of the driving stage are connected capacitors forming a resonance tank.

The final stage has the same structure like the driving stage but with much bigger

transistors for 500 mA switching current. The secondary winding of the output transformers X9, X10 and X11, X12 are connected in series with VEE on top and on the bottom; the output is centered between X10 and X11.

Each stage of the power amplifier operates in class-AB to get as high as possible power added efficiency from the linear class of the operation.

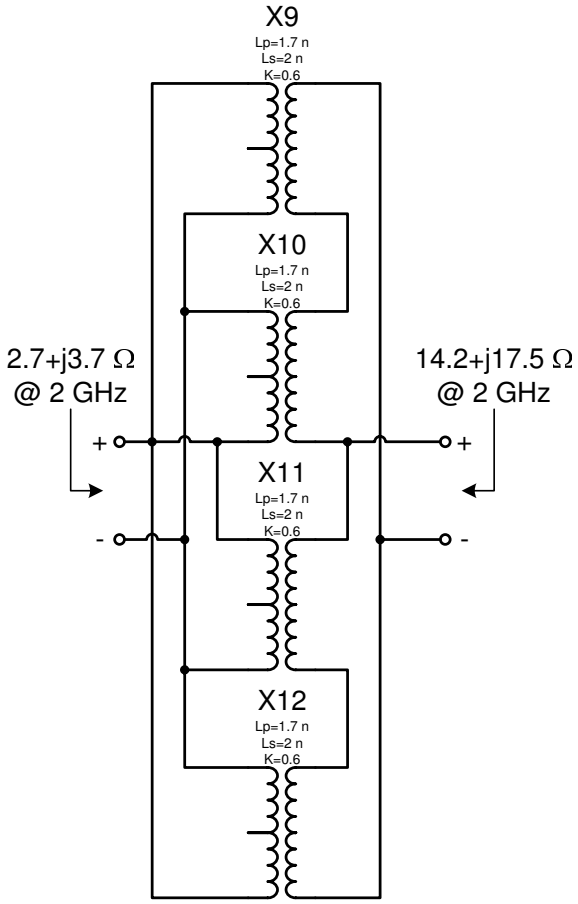
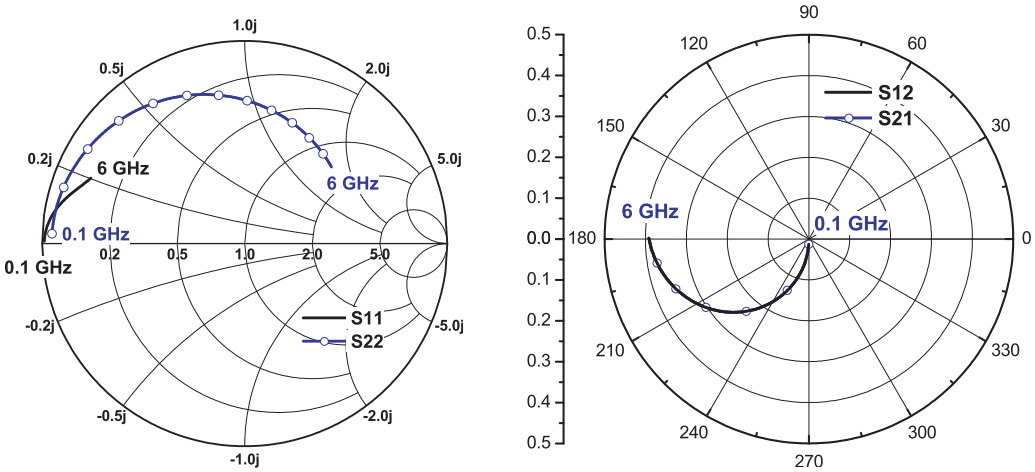


Figure 5.43: Output power combining transformer connection for the S-parameter simulation.

Fig. 5.43 shows a connection scheme of the inputs and outputs of the power combining transformer for the differential S-parameter simulation. The simulated S-parameters for the frequency range from 0.1 GHz to 6 GHz are shown in Fig. 5.44.

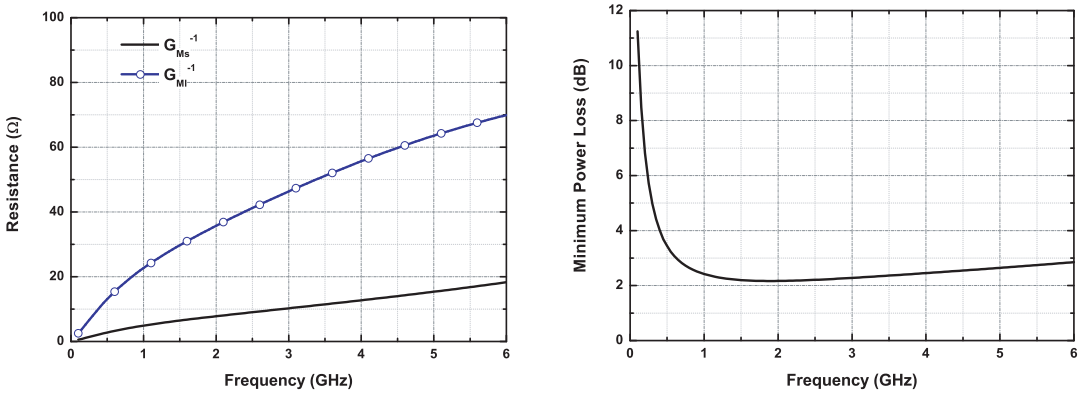
The output transformer has a minimum power loss of 2.2 dB at the frequency of 2 GHz (see Fig. 5.45(b)). The required input and output parallel impedances for the simultaneously match condition versus frequency are shown in Fig. 5.45(a).

The output matching network (see Fig. 5.46) has a power loss of 2.35 dBm. The frequency dependency of the output matching network power loss is shown in Fig. 5.47(b). The impedance delivered to each power amplifier is a four times



(a) (b)

Figure 5.44: S-parameters of the output power combining transformer: (a) S11, S22; (b) S12, S21.



(a) (b)

Figure 5.45: Simulation results of the output power combining transformer: (a) Parallel source and load resistances required for the simultaneous conjugate match condition; (b) Minimum power loss.

higher than the input impedance shown in Fig. 5.47(a) and equals to 13.3+j15.1 Ω at 2 GHz.

The chip photo of the implemented power amplifier in a 28 GHz-f_t SiGe-bipolar technology is shown in Fig. 5.48. One cell of the output transformer has a size of 585 μm x 585 μm.

Output load-pull measurements were made for 1.95 GHz and 2.44 GHz to find an optimum impedance for highest power added efficiency. Fig. 5.49 shows the output power and the corresponding power added efficiency for 50 Ω (solid line) input- and output impedance. The amplifier shows a very flat frequency response concerning the output power at moderate efficiency. The efficiency can be in-

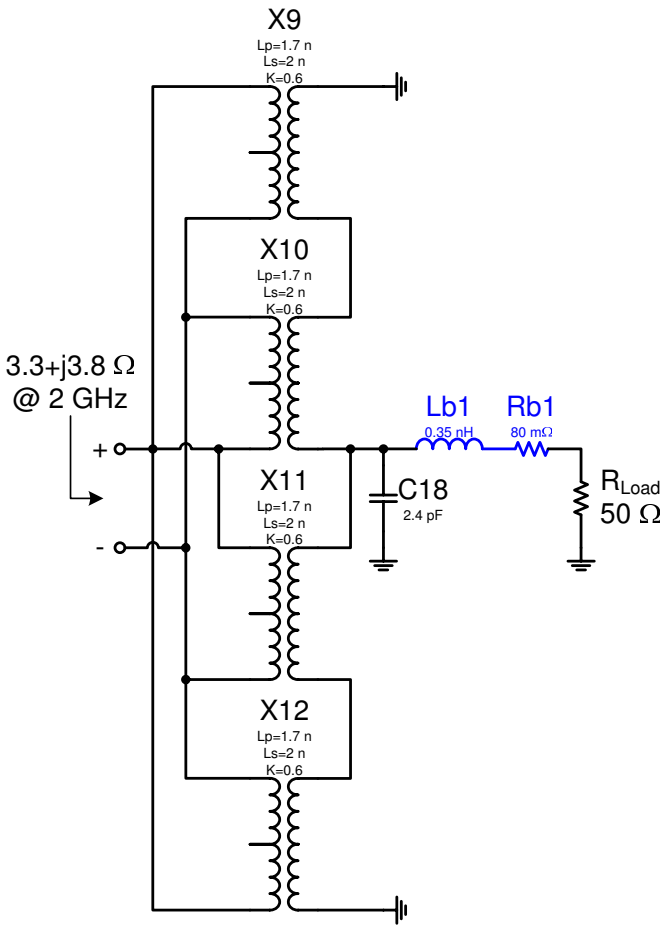
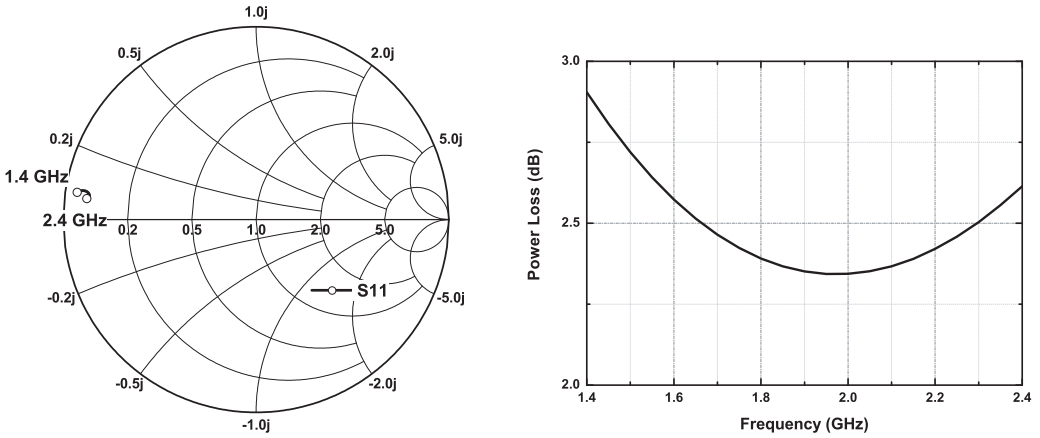


Figure 5.46: Circuit diagram for the power combining transformer-based output matching network simulation.

creased in a narrow band by simple output prematching at one frequency. In the present work the prematching at two frequencies (1.95 GHz and 2.44 GHz) were observed. In Fig. 5.49 we can see the measured frequency responses of the output power and the power added efficiency (PAE) for three different output impedances. The following maximum output power and PAE with different load impedances was achieved: 31.6 dBm and 24.6 % PAE at 1.79 GHz (solid line) for 50 Ω microstrip line; 31.1 dBm and 29.2 % PAE at 1.93 GHz (dotted line) for prematching to 21.5+j11.5 Ω at 1.95 GHz; 32.3 dBm and 30.6 % PAE at 2.12 GHz (dashed line) for prematching to 17.2+j7.3 Ω at 2.44 GHz. The power transfer characteristics for both prematching cases are shown in Fig. 5.50. All measurements were made at 3.5 V supply voltage.



(a) (b)

Figure 5.47: Simulation results of the output matching network: (a) S11; (b) Power loss.

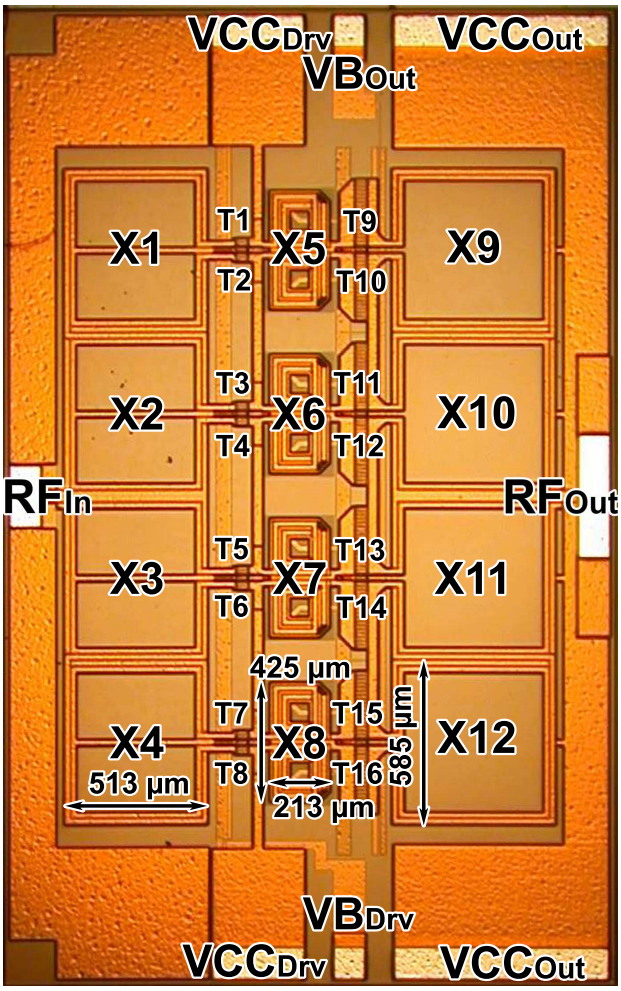


Figure 5.48: Die photograph of the power amplifier (size 3.5 mm x 2.2 mm).

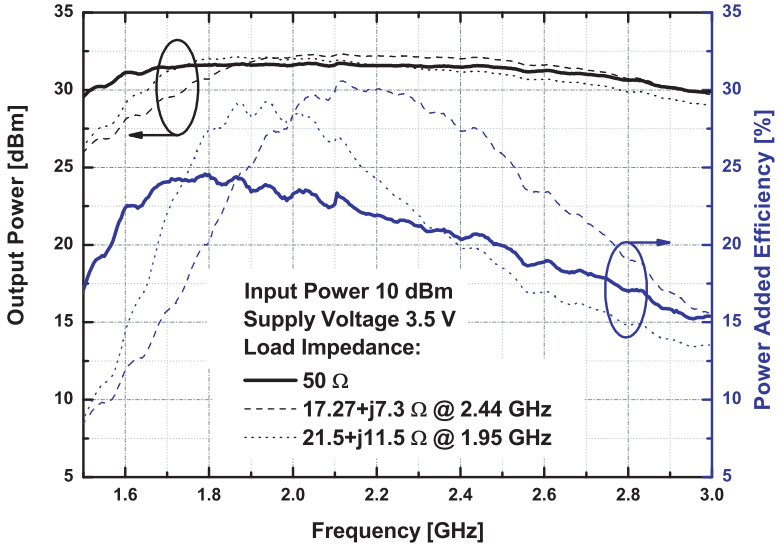


Figure 5.49: Measured frequency responses of the power amplifier.

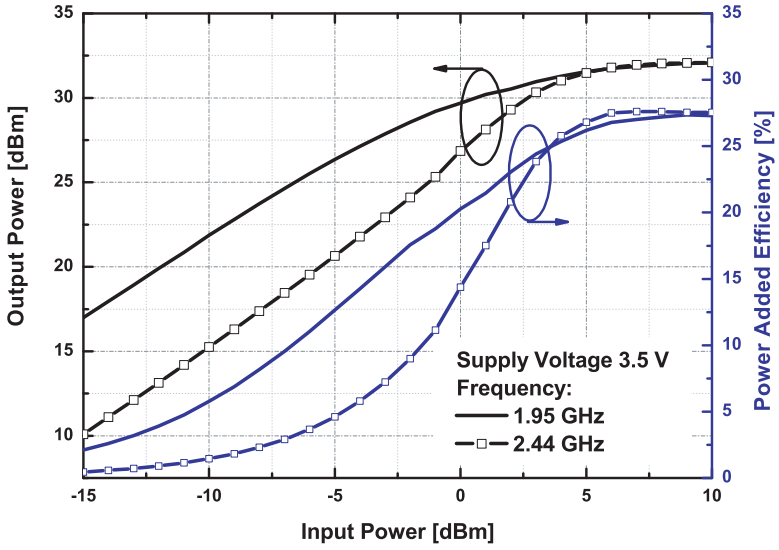


Figure 5.50: Measured power transfer characteristics of the power amplifier.

Chapter 6

Conclusion and Outlook

Conclusion

The III-V and SiGe-bipolar technologies still dominate at the microwave power amplifier market. Up to date, modern standard digital CMOS technologies (0.13 μm, 0.18 μm) were not considered as the mass production technologies for the mobile microwave power amplifier development. But the reality is that just a power amplifier implemented in a standard digital CMOS process can be integrated in a chip with other components of the modern mobile communication system. This leads to the goal of this work which is to verify the feasibility and to determine the performance limit of the fully monolithically-integrated Class-AB push-pull transformer-based power amplifier architecture for the current and future mobile applications in a standard digital 0.13 μm CMOS technology. Besides, several similar power amplifiers were implemented in a modern 0.35 μm SiGe-Bipolar technology.

The main results of this work are listed below:

- A 2.4 GHz power amplifier in 0.13 μm CMOS technology. An output power of 28 dBm is achieved with a power added efficiency of 48 % at a supply voltage of 1.2 V [Vasylyev 04].
- Two 17 GHz power amplifiers in 0.13 μm CMOS technology (one fully integrated while the other with external matching network) with output power exceeding 50 mW. The former exhibits a power added efficiency of 9.3 % while the latter a 15.6 % power added efficiency [Vasylyev 06].
- A fully integrated K and Ka bands power amplifier in 0.13 μm CMOS technology. A 13 dBm output power along with power added efficiency of 13 % is achieved at an operating frequency of 25.7 GHz with 1.2 V supply [Vasylyev 05,a].
- A fully integrated power amplifier based on a novel power combining transformer structure in 28 GHz-f_T SiGe-bipolar technology. A 32 dBm output

power along with power added efficiency of 30 % is achieved at an operating frequency of 2.12 GHz with 3.5 V supply [Vasylyev 05,b].

Outlook

The technology development is driven by the digital CMOS components like microprocessors, DSP's and DRAM's. They push the performance of the active device to a smaller size, higher transit and maximum oscillation frequencies. But along with it newer devices have a lower breakdown voltage, new physical effect causes that devices behave more far from the desired or "ideal" one, the metal layers becomes thinner and in a case of a high integration system (one chip solution) the heat dissipation per area increases the operating temperature and as result degrades the active and passive device performances.

Hence, circuit design solutions like a cascode configuration, stack architecture etc. will spend all advantages of newer technologies to overcome their drawbacks. But still to create a competitive fully monolithically integrated power amplifier a low resistive (thick), high electromigration current density metallization layers are desired.

Appendix A

Power Amplifier State of the Art

In this Appendix the interested publications of the last decade are collected and sectioned in three parts: the power amplifiers in III - V technologies (see Table A.1), the power amplifier in CMOS technologies (see Table A.2) and the power amplifiers in Si, SiGe - Bipolar technologies (see Table A.3).

Table A.1: Published (state of the art) power amplifiers in III-V technologies.

Reference	**f [GHz]**	η [%]	**Gain$_{S-s}$ [dB]**	**P$_{Out}$ [dBm]**	**Supply [V]**	**Class**	**Technology**	**Integration**
[Paidi 05]	172	5_{PAE}	5	8.3	2.1		InP DHBT	Unbalanced, FI
	176	3_{PAE}	6.5	9	2.05		InP DHBT	Unbalanced, FI
	84	13_{PAE}	6.5	15.1	2.25		InP DHBT	Unbalanced, FI
	92	10_{PAE}	5	13.7	2.25		InP DHBT	Unbalanced, FI
[Akkul 04]	1.8	76_{PAE}		42	12	F	$0.5\mu m$ PHEMT	Unbalanced, OCM
[Bahl 04]	6.5	45_{PAE}	15	33	8	AB	MSAG MESFET GaAs	Unbalanced, FI
[Behtash 04,b]	10	32_{PAE}	10	34.2	25	AB	HEMT AlGaN/GaN	Unbalanced, FI
[Behtash 04,a]	10	36.7_{PAE}	10	37.2	20	AB	HEMT AlGaN/GaN	Unbalanced, FI
[Chu 04]	10	$33.7_{PAE_{2dB}}$	17.5	39.3_{2dB}	8	A	PHEMT GaAs	Unbalanced, FI
[Chung 04]	2.1	40_{PAE}	12	50	28	AB	MRF21030 LDMOS	Unbalanced, OCM
[Dow 04]	2.44	100mA@ EVM=4.2	29.4@ EVM=4.2	20@ EVM=4.2	3.3		InGaP/GaAs	Unbalanced, OCM
	5.2	201mA@ EVM=4.2	16@ EVM=4.2	23@ EVM=4.2	4.5			
	5.5	170mA@ EVM=3.9	24@ EVM=3.9	19@ EVM=4.2	3.3			
[Eccleston 04]	1.65	40_{PAE}	7.3	24.7	5.5	B DFDA	FLK012WF FET GaAs	Unbalanced, OCM
[Ellis 04]	94.5	¡5.3	8.5	14.4	4	A	InP DHBT	Unbalanced, FI
[Fujii 04]	18-28	$18_{PAE_{1dB}}$	20	30_{1dB}	5		FET PHEMT	Lange coupler, FI
	26-32	$16_{PAE_{1dB}}$	20	29_{1dB}	5		FET PHEMT	Lange coupler, FI
	37-42	$14_{PAE_{1dB}}$	20	28.5_{1dB}	5		FET PHEMT	Lange coupler, FI
[Fukuda 04]	0.9/ 1.9	46_{PAE}/ 62_{PAE}	16/ 17.4	30.8/ 31	8		FET GaAS	Unbalanced, OCM, MEMS
[Gruendlingh 04]	5.25	80		30	5	F Chireix	GaAs PHEMT	Unbalanced, OCM
[Kunihiro 04]	2.4/ 5.25	40_{PAE}/ 22_{PAE}	34/ 25	29/ 27	3.3		InGaP/GaAs HBT	Unbalanced, LTCC
[Noh 04]	2.4	$42_{PAE_{1dB}}$	24.4	27_{1dB}	3.3		InGaP/GaAs HBT	Unbalanced, OCM
	5.2	$31.2_{PAE_{1dB}}$	14.8	27.2_{1dB}				
[Ooi 04]	0.9	71.4_{PAE}	14	22	3	F	PHEMT	Unbalanced, OCM
[Samoska 04]	150	3_{PAE}	13	13	2		InP HEMT	Unbalanced FI

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Reference	f [GHz]	η [%]	Gain_{S-s} [dB]	P_{Out} [dBm]	Supply [V]	Class	Technology	Integration
[Upshur 04]	2.2 8.4	65_{PAE} 47.2_{PAE}	18 8	27 34.9	7 7	E or F E or F	PHEMT PHEMT	
[Ooi 04]	10	51_{PAE}	10	20.3	4	E	MESFT GaAs	Unbalanced, OCM
[Yamamoto 04]	5	$30_{PAE_{1dB}}$	23.2	23.2_{1dB}	3	AB	HBT InGaP/GaAs	Unbalanced, RFC, OCM
[Wang 04,b]	10	67	9.5	20.3	4	E	GaAs MESFET	Unbalanced, OCM

Table A.2: Published (state of the art) power amplifiers in CMOS tecnologies.

Reference	f [GHz]	η [%]	Gain_{S-s} [dB]	P_{Out} [dBm]	Supply [V]	Class	Technology	Integration
[Vasylyev 06]	17.2 17.2	15.6_{PAE} 9.3_{PAE}	11.5 14.5	17.8 17.1	1.5 1.5	AB AB	$0.13\mu m$ CMOS	Balanced, OCM Balanced, FI
[Vasylyev 05,a]	25.7	13.2_{PAE}	8.4	13	1.5	AB	$0.13\mu m$ CMOS	Balanced, FI
[Ellinger 05]	$10 \div 59$		9.7 ± 1.6	12.5@ 20GHz	2	A	$0.09\mu m$ SOI CMOS	Unbalanced, FI, Travelling-Wave
[Vasylyev 04]	2.4	48_{PAE}	26	28	1.2	AB	$0.13\mu m$ CMOS	Balanced, OCM
[Ding 04]	5	44_{PAE}	12	22		A‖B	$0.18\mu m$ CMOS	Balanced, FI, Balun is required
[Eo 04,a]	2.4 5.2	$15.3_{PAE_{1dB}}$	3.7 24	9.7 19.5		AB AB	$0.18\mu m$ CMOS	Unbalanced, RFC is required
[Eo 04,c]	5	$17.5_{PAE_{1dB}}$	7.1	19.2_{1dB}	1.8	AB linearized	$0.18\mu m$ CMOS	Unbalanced, RFC is required
[Tu 04]	0.835	65		26.5	2.4	E linearized	CMOS	
[Chee 04]	1.92	38	25	6.8	1.5	AB	$0.13\mu m$ CMOS	Unbalanced, OCM
[Zhang 04]	0.9		30	26	1.8	AB linearized	$0.18\mu m$ CMOS	Balanced
[Grewing 04]	8_{3dB}		17	3.5_{1dB}	2		$0.13\mu m$ CMOS	Distributed, FI
[Wang 04,a]	1.75	23_{PAE}	21	24	3.3	AB linearized	$0.5\mu m$ CMOS	Unbalanced, RFC required.
[Wang 04,c]	5.2	32_{PAE}	27	19.5	1.8	AB	$0.18\mu m$ CMOS	Balanced, FI
[Eo 04,b]	5	20_{PAE}	21	24.1	1.8	AB	$0.18\mu m$ CMOS	Balanced, Balun&RFC required
[Komijani 04]	24	11	7	14.5	2.8	AB	$0.18\mu m$ CMOS	Unbalanced, FI
[Toner 04]	5.5	$9.3_{PAE_{1dB}}$	6.7	-3.3_{1dB}	1.8	A linearized	$0.18\mu m$ CMOS	Unbalanced, OCM
[Sowlati 02] [Sowlati 03]	2.4	42_{PAE}	38	23	2.4	AB self biased	$0.18\mu m$ CMOS	Unbalanced, OCM
[Ho 03]	2.45	35_{PAE}		20	1.2	E	$0.35\mu m$ CMOS	Balanced, BW, Balun Required
[Thueringer 03]	17		11	5_{1dB}	1.5	A	$0.13\mu m$ CMOS	Balanced, FI, Balun Required
[Hamedi-Hagh 03]	8	38_{PAE}		20	1	F	$0.18\mu m$ CMOS	Unbalanced, FI
[Yen 03]	2.4	28_{PAE}	11.2	20_{1dB}	2.5	AB linearized	$0.25\mu m$ CMOS	Unbalanced, OCM
[Khannur 03]	2.45	16_{1dB}	12.5	3.5_{1dB}	1.8	AB	$0.18\mu m$ CMOS	Unbalanced, FI After T/R switch
[Point 03]	2.4	$29_{PAE_{1dB}}$	7.5	23_{1dB}	1.8	AB	$0.25\mu m$ CMOS	Balanced, OCM
[Hung 03]	1.2 2.65	62_{PAE} 38_{PAE}		26 25.5	1.3 1.7	E E	$0.25\mu m$ CMOS $0.35\mu m$ CMOS	Balanced, BW Balanced, Balun Required
[Aoki 03]	1.9	50_{PAE}	27	34.5	1.8	F	$0.18\mu m$ CMOS	Balanced, FI
[Mertens 02]	0.7	62_{PAE}		30	2.3	E	$0.35\mu m$ CMOS	Balanced, BW, Balun Required
[Hella 02]	2	33_{PAE}		16	3.3	AB	$0.35\mu m$ CMOS	Unbalanced, BW
[Ho 02]	2.4	35_{PAE}		20	1.2	E	$0.35\mu m$ CMOS	Balanced, BW, Balun is required
[Fallesen 01,a]	1.73	45_{PAE}		30.4	3	AB	$0.35\mu m$	Unbalanced,

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Reference	**f [GHz]**	η **[%]**	**Gain$_{S-s}$ [dB]**	**P$_{Out}$ [dBm]**	**Supply [V]**	**Class**	**Technology**	**Integration**
							CMOS	BW
[Fallesen 01,b]	1.75	55_{PAE}		30.4	3	AB	0.35μm CMOS	Unbalanced, BW
[Yoo 01]	0.9	41_{PAE}		29.54	1.8	E	0.25μm CMOS	Balanced, BW, Balun is required
[Heo 01]	1.9	48_{PAE}	17	26	3.3	AB	0.8μm BiCMOS	Unbalanced, LTCC
[Fortes 01]	1.9	42_{PAE}	10.5	22.8	3	F	0.6μm CMOS	Unbalanced, BW
[Shirvani 02] [Shirvani 01]	1.4	49_{PAE}		24.8	1.5	Parallel F	0.25μm CMOS	Unbalanced, BW
[Aoki 02,a] [Aoki 02,b]	2.4	41_{PAE}	8.7	32.78	2	F	0.35μm BiCMOS	Balanced, FI, Balun is required
[Aoki 01]	2.4	31_{PAE}	8.5	33.4	2	F		Balanced, FI
[Hella 01]	1.85	30_{PAE}		16.5	3.3	AB	0.35μm CMOS	Unbalanced, OCM
[Wang 01]	1.9	40_{PAE}	7	20	3.3	AB	0.6μm CMOS	Unbalanced, FI
[Baureis 01]	1.1	31_{PAE}	10	21	4.5	AB	0.6μm CMOS	Unbalanced, FI
[Chen 01]	2.4	31_{PAE}	10	20	2.5	AB	0.24μm CMOS	Unbalanced, FI, MSI
[Hsiao 01]	2.4	16_{PAE}	13.9	17.5	5	A	0.35μm CMOS	Unbalanced, FI
[Kim 01]	0.9	45_{PAE}		20	2.8	D?	0.35μm CMOS	Balanced, OCM
[Kuo 01]	0.9	43_{PAE}		31.76	3	F	0.2 μm CMOS	Balanced, OCM
[Gupta 01]	0.9	30_{PAE}		19.3	3	C	0.6 μm CMOS	Balanced, FI, Balun is required
[Yamamoto 01]	2.4	$> 19_{PAE}$	20	> 9	1.8	AB	0.18 μm CMOS	Unbalanced, OCM
[Suematsu 01]	5	37_{PAE}	6.2	14	1.8	AB CPP	0.18 μm CMOS	Unbalanced, BW
[Giry 00]	1.9	35_{PAE}	15	23.5	2.5	AB	0.35 μm CMOS	Unbalanced, RFC, Off-chip capacitors
[Yoo 00]	0.9	41.4_{PAE}		30	1.9	E	0.25 μm CMOS	Unbalanced, BW Off-chip capacitors
[Sutono 00]	1.9	40_{PAE}	16	25		F	0.8 μm CMOS	Unbalanced, LTCC
[Asbeck 00]	1.9	27.4_{PAE}	20.7	29	3	B	0.25 μm CMOS	Unbalanced, Off-chip
[Chen 00]	1.9 1.9 2.4	16_{PAE} 32_{PAE} 44_{PAE}		20 24 22	3 3 2.5		0.8 μm CMOS 0.24 μm CMOS	Unbalanced, FI Unbalanced, LTCC Unbalanced, OCM
[Tsai 99]	1.9	48_{PAE}		30	2	E	0.35 μm CMOS	Balanced, FI Balun is required
[Gupta 98]	0.9	50		20		C	0.5 μm CMOS	Balanced, FI Balun is required
[Su 97]	0.835	42_{PAE}	30	30	2.5	D	0.8 μm CMOS	Unbalanced, OCM
[Rofougaran 94]	0.9	30_{PAE}	30	17	3	C	1 μm CMOS	Balanced, OCM

Table A.3: Published (state of the art) power amplifiers in Si, SiGE-Bipolar tecnologies.

Reference	f [GHz]	η [%]	Gain_{S-s} [dB]	P_{Out} [dBm]	Supply [V]	Class	Technology	Integration
[Vasylyev 05,b]	2.12	30_{PAE}	32	32.3	3.5	AB	28GHzf_T SiGeBipolar	Balanced, FI
[Scuderi 05]	1.8	46_{PAE}	32	33.5	3.5	C-E	0.8μm SiBiPMOS	Unbalanced, OCM
[Bakalski 04,b]	5.25	30_{PAE}	27	25.9	3.3		40GHzf_T SiGeBipolar	Unbalanced, OCM
[Bakalski 04,a]	2.45 5.25	42.8_{PAE} 30_{PAE}	31 26	29 25.9	3.3 3.3		42GHzf_T SiGeBipolar	Unbalanced, OCM
[Scuderi 04,b]	5.2	26_{PAE}	24	25	3	C-E	0.8μm SiBipolar	Unbalanced, OCM
[Scuderi 04,c]	2.5	52_{PAE}	30	26_{1dB}	3.3	C-E	0.8μm SiBipolar	Unbalanced, OCM
[Scuderi 04,a]	1.8	50_{PAE}	32	33.8	3.5	C-E	0.8μm SiBiPMOS	Unbalanced, OCM
[Johnson 04]	0.9 1.8	55_{PAE} 45_{PAE}		34.5 31.5	3.5 3.5		SiGe BiCMOS SiGe BiCMOS	LTCC LTCC
[Deng 04] [Deng 05]	1.95	31_{PAE}	13	25.9_{1dB}		AB linearized	0.25μm SiGe BiCMOS	Unbalanced, OCM
[Kitlinski 04]	1.95	50_{PAE}	32	29	3.3	AB	0.35μm SiGe Bipolar	Unbalanced, OCM
[Pfeiffer 04]	77	2.5_{PAE}	6.1	11.6_{1dB}	2.5	AB	0.12μm SiGe Bipolar	Balanced, FI, Balun is required
[Bakalski 03,a]	5.9	36_{PAE}	23	24.8	2.4	AB	40GHzf_T BiCMOS	Balanced, OCM, LTCC
[Bakalski 03,c]	5.8	14.2_{PAE}	23	20.7	2	AB	38GHzf_T BiCMOS	Balanced, FI
[Bakalski 03,b] [Bakalski 04,c]	5.3	24_{PAE}	26	25	2.4	AB	0.25μm SiGeBipolar	Balanced, FI
[Bakalski 03,d]	17.2	10.1_{PAE}	15	17.5	2.4	AB	75GHzf_T SiGe BiCMOS	Balanced, FI
[Rippke 03]	1.95	30_{PAE}	24	24	3.3	AB	SiGe BiCMOS	Unbalanced, FI
[OSullivan 03]	2.2	25_{PAE}	13	9	1.3	F	0.8μm BiCMOS	Unbalanced, FI
[Tanzi 03]	5	24_{PAE}	20.6	31.5			0.35μm BiCMOS	Balanced, LTCC
[Juurakko 03]	2	18.5_{PAE}	22	26.7	2.7		0.35μm SiGe BiCMOS	Balanced, OCM
[Juurakko 03]	2	18.5_{PAE}	22	26.7	2.7		0.35μm SiGe BiCMOS	Balanced, OCM
[Shinjo 03]	5.8		19.6	15.3_{1dB}		Self biased	SiGe HBT	Unbalanced, FI
[Scuderi 03]	1.8	51_{PAE}	33	33	3	C-E	0.8μm SiBiPolar	Unbalanced, OCM
[Bakalski 02]	2.45	46_{PAE}	35	29.1	3	AB	25GHzf_T SiBipolar	Balanced, OCM, Balun is required
[Carrara 02,a] [Carrara 02,b]	1.8	57_{PAE}	33	34	2.7	C-E	0.8μm SiBipolar	Unbalanced, OCM
[Raghavan 02]	2.4	47_{PAE}	35	27.5	3.3	F-like	SiGe HBT	Unbalanced, LTCC
[Luo 01,a] [Luo 01,b]	1.9	30_{PAE}	21.5	28.2	3.6	Self controlled	30GHzf_T BiCMOS	Unbalanced, OCM
[Bischof 01]	0.9 1.8	58_{PAE} 48_{PAE}	40 30	35 33	3.5 3.5		22GHzf_T SiGe HBT	Unbalanced, Off-chip
[Heinz 00]	0.9 0.9	54_{PAE} 57_{PAE}	38 38	35 38.86	2.8 4.5	AB AB	0.8μm SiBipolar	Balanced, OCM, Balun is required
[Simbuerger 00]	1.9	55_{PAE}	28	31.5	3	AB	0.5μm SiBipolar	Balanced, OCM, Balun
[Zhang 00]	1.88	52_{PAE}	20	33	3.4		8-inch SiGeBCMOS	Unbalanced, OCM
[Tseng 00]	0.84	51_{PAE}	21	31	3		SiGe HBT	Unbalanced, OCM
[Chan 99]	0.9	11.7_{PAE}	16	17	3	C	0.8μm BiCMOS	Unbalanced, FI, RFC is required
[Simbuerger 99,b] [Simbuerger 99,a]	0.9	59_{PAE}	35	35.5	3.6	AB	0.8μm SiBipolar	Balanced, OCM, Balun is required
[Cartalade 98]	2	25_{PAE}	22	20	3	AB	0.5μm	Balanced,

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Reference	**f [GHz]**	η **[%]**	**Gain$_{S-s}$ [dB]**	**P$_{Out}$ [dBm]**	**Supply [V]**	**Class**	**Technology**	**Integration**
							BiCMOS	OCM, Balun is required
[Trost 97]	1.9 1.9	26.3_{PAE} 31.5_{PAE}	40 40	32 28	6 3.3	AB AB	$0.8\mu m$ SiBipolar	Balanced, OCM, Balun is required
[Simbuerger 96]	1.9 2.4	33_{PAE} 23_{PAE}	34 33	31.1 30	5 6	AB AB	$0.8\mu m$ SiBipolar	Balanced, OCM, Balun is required
[Wong 96]	0.83	30_{PAE}	30	30	5	AB	$0.8\mu m$ BiCMOS	Unbalanced, OCM
[Erben 95]	5.7	$30_{PAE_{1dB}}$	7.5	20_{1dB}	4	A	SiGe HBT	Transistor test

Appendix B

I-V characteristic in the BSIM4 model

In this Appendix a background of the BSIM4 single equation I-V characteristic at the strong inversion region is given.

The drain current of the MOS transistor for the strong inversion region is usually split into two regions (the triode and saturation) and is expressed as:

$$I_d = \begin{cases} \frac{W}{L}\mu_n C'_{ox}\left[(V_{gs}-V_{th})\,V_{ds} - \frac{1}{2}(1+\delta)V_{ds}^2\right] & V_{ds} \le V_{dsat} \\ \frac{1}{2}\frac{W}{L}\mu_n C'_{ox}\frac{(V_{gs}-V_{th})^2}{1+\delta} & V_{ds} > V_{dsat} \end{cases} \tag{B.1}$$

where

$$V_{dsat} = \frac{V_{gs}-V_{th}}{1+\delta} \tag{B.2}$$

and δ is the bulk-charge factor.

Such modelling of the drain current leads to kinks and discontinuities in the device characteristics and their derivatives that gives a numerical difficulty during a simulation.

To overcome the discontinuities and kinks, the smoothing functions (V_{gsteff}, V_{dseff} etc.), which merge the multiple equation description of the MOS device into a single ∞-differentiable equation, are applied in the BSIM4 model. The drain current without including the source/drain resistance and CLM, DIBL, SCBE, DITS effects in accordance with the BSIM4 model is expressed as:

$$I_d = \frac{W_{eff}\cdot\mu_{eff}\cdot C'_{ox,IV}}{L_{eff}\left[1+(\mu_{eff}V_{dseff})/(2VSAT\cdot L_{eff})\right]}\cdot V_{gsteff}\cdot V_{dseff}\cdot(1-V_{dseff}/2V_b) \tag{B.3}$$

where

$$V_b = \frac{V_{gsteff} + 2kT/q}{A_{bulk}}; \tag{B.4}$$

A_{bulk} is a factor to describe the bulk charge; $C'_{ox,IV}$ is an effective oxide capacitance for I-V calculation; L_{eff}, W_{eff}, μ_{eff} are an effective channel length, channel width and mobility; and $VSAT$ is a saturation velocity.

The effective drain-to-source voltage (V_{dseff}) smoothes out the transition between the triode and saturation regions, is expressed as:

$$V_{dseff} = V_{dsat} - \frac{1}{2}\left(V_{dsat} - V_{ds} - DELTA + \sqrt{(V_{dsat} - V_{ds} - DELTA)^2 + 4DELTA \cdot V_{dsat}}\right) \tag{B.5}$$

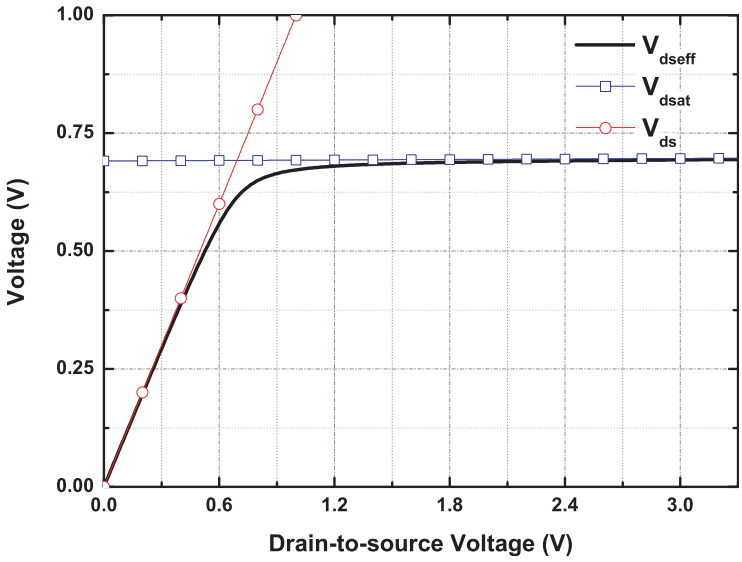

Figure B.1: The effective drain-to-source voltage (V_{dseff}).

Fig. B.1 shows if $V_{ds} < V_{dsat}$ then V_{dseff} approaches V_{ds} and when $V_{ds} > V_{dsat}$ then V_{dseff} approaches V_{dsat}. The BSIM4 model has a quite complex equation for the saturation voltages (V_{dsat}) but for this analysis the simplification (B.2) is used instead.

The simplified equation for the effective V_{gsteff} smoothing function that smoothes out the transition between the subthreshold and strong inversion regions, is given by:

$$V_{gsteff} = \frac{2nKt/q \ln\left[1 + \exp\left(\frac{V_{gseff} - V_{th}}{2nKt/q}\right)\right]}{1 + 2n\exp\left(-\frac{V_{gseff} - V_{th} - 2V_{off}}{2nkT/q}\right)} \tag{B.6}$$

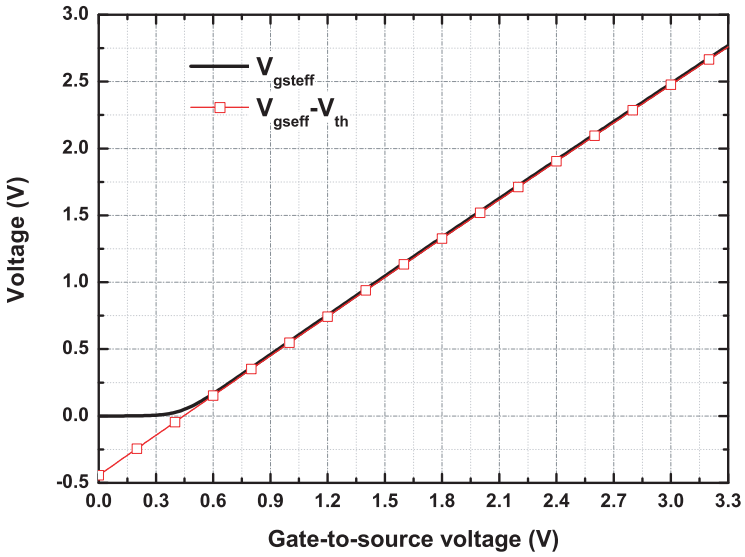

Figure B.2: The effective $V_{gseff} - V_{th}$ function (V_{gsteff}).

Fig. B.2 shows that for the strong inversion region ($V_{gseff} > V_{th}$) the effective V_{gsteff} function approaches $V_{gseff} - V_{th}$. The BSIM4 model takes into account poly-depletion effects by subtracting a voltage drop across the polysilicon gate $V_{polyeff}$ from the gate-source voltage V_{gs}:

$$V_{gseff} = V_{gs} - V_{polyeff} \tag{B.7}$$

The poly-depletion effects are neglected and V_{gs} voltage is used instead in the text below .

The substitution of the V_{gsteff} and V_{dseff} values at the triode and strong inversion regions in to (B.3) gives:

$$\begin{aligned} I_d &= \frac{W_{eff}}{L'_{eff}} \cdot \mu_{eff} \cdot C'_{ox,IV} \cdot (V_{gseff} - V_{th}) \cdot V_{ds} \cdot (1 - V_{ds}/2V_b) \\ &= \frac{W_{eff}}{L'_{eff}} \cdot \mu_{eff} \cdot C'_{ox,IV} \cdot (V_{gs} - V_{th}) \cdot V_{ds} \cdot \left(1 - \frac{A_{bulk} V_{ds}}{2(V_{gs} - V_{th} + 2kT/q)}\right) \\ &= \frac{W_{eff}}{L'_{eff}} \cdot \mu_{eff} \cdot C'_{ox,IV} \left((V_{gs} - V_{th})\, V_{ds} - \frac{A_{bulk}\,(V_{gs} - V_{th})\, V_{ds}^2}{2(V_{gs} - V_{th} + 2kT/q)}\right) \end{aligned} \tag{B.8}$$

where

$$L'_{eff} = L_{eff} \left(1 + \frac{\mu_{eff} V_{dseff}}{2VSAT \cdot L_{eff}}\right) \tag{B.9}$$

Since $2kT/q$ is a small number and as a first approximation A_{bulk} equals to $1 + \delta$, (B.8) is equated to the top equation of (B.1):

$$I_d = \frac{W_{eff}}{L'_{eff}} \cdot \mu_{eff} \cdot C'_{ox,IV} \left[(V_{gs} - V_{th})\, V_{ds} - \frac{1}{2}(1+\delta) V_{ds}^2 \right] \tag{B.10}$$

The substitution of the V_{gsteff} and V_{dseff} values at the saturation and strong inversion regions in to (B.3) gives:

$$I_d = \frac{1}{K} \frac{W_{eff}}{L'_{eff}} \cdot \mu_{eff} \cdot C'_{ox,IV} \cdot \frac{(V_{gs} - V_{th})^2}{1+\delta} \tag{B.11}$$

where

$$K = \frac{1}{(1 - V_{dseff}/2V_b)} \tag{B.12}$$

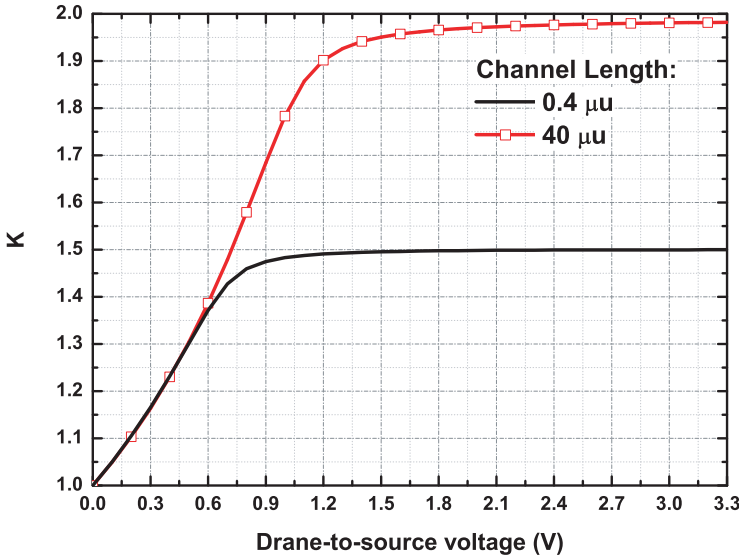

Figure B.3: K multiplier.

The multiplier K approaches the value of 2 for the long channel devices at the saturation (see Fig. B.3) that finally transforms (B.11) to the bottom equation of (B.1).

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